[File 60] **ANTE: Abstracts in New Tech & Engineer** 1966-2007/Jul

[File 56] **Computer and Information Systems Abstracts** 1966-2007/Aug

[File 35] **Dissertation Abs Online** 1861-2007/Jul

[File 8] **Ei Compendex(R)** 1884-2007/Aug W1

[File 266] **FEDRIP** 2007/Jul

[File 583] **Gale Group Globalbase(TM)** 1986-2002/Dec 13

File 583: This file is no longer updating as of 12-13-2002.
[File 65] **Inside Conferences** 1993-2007/Aug 15

[File 2] **INSPEC** 1898-2007/Aug W1

[File 6] **NTIS** 1964-2007/Aug W3

[File 144] **Pascal** 1973-2007/Jul W5

[File 34] **SciSearch(R) Cited Ref Sci** 1990-2007/Aug W3

[File 434] **SciSearch(R) Cited Ref Sci** 1974-1989/Dec

[File 256] **TecInfoSource** 82-2007/Nov

[File 95] **TEME-Technology & Management** 1989-2007/Aug W2

[File 99] **Wilson Appl. Sci & Tech Abs** 1983-2007/Jul

Set Items Description
S1 4805 S (STEINER(1W)(TREE? ? OR NODE OR POINT? ? OR VERTICE? ?)) OR (S()STEINER(1W)(TREE? ? OR NODE OR POINT? ? OR VERTICE? ?)) OR NASH()WILLIAMS()TUTTE(2N)THEOR????? OR ((NASH(1W)WILLIAMS(1W)TUTTE)(2N)THEOR?????)
S2 6299 S ((STEINER(1W)TREE? ? OR TREE? ? OR NODE OR POINT? ? OR VERTICE? ?)(5N)(SET OR SUBSET OR SUB()SET))(10N)(NODE OR STRUCTURE? ?)
S3 281340 S ((STEINER(1W)TREE? ? OR TREE? ? OR NODE OR POINT? ? OR VERTICE? ?)(10N)(CLIENT? ? OR ENTIT??? OR NODE))
S4 291 S S1(20N)(CREAT??? OR GENERAT???)
S5 347 S (S1(10N)(MERG??? OR PACK??? OR TOGETHER OR MIX??? OR BLEND??? OR BINDING OR BOUND OR COMBIN??? OR CONSOLIDAT??? OR COMPRESS??? OR CONDENS??? OR JOIN?????))
S6 203 RD (unique items)
S7 250 S (S1(5N)(MERG??? OR PACK??? OR TOGETHER OR MIX??? OR BLEND??? OR BINDING OR BOUND OR COMBIN??? OR CONSOLIDAT??? OR COMPRESS??? OR CONDENS??? OR JOIN?????))
S8 4444 S (STEINER(1W)TREE? ?)
S9 143 S (S8(5N)(MERG??? OR PACK??? OR TOGETHER OR BINDING OR COMBIN??? OR CONSOLIDAT??? OR JOIN?????))
S10 78 RD (unique items)
S11 0 S S10 AND AC=US/PR AND AY=(1963:2003)/PR
S12 0 S S10 AND AC=US AND AY=1963:2003
S13 0 S S10 AND AC=US AND AY=(1963:2003)/PR
S14 54 S S10 AND PY=1963:2003
S15 0 S S10 AND NOTPY=2003:2007
S16 47 S S10 NOT PY=2003:2007
S17 0 S S16 AND (AU=(JAIN, K? OR JAIN K?))
S18 0 S S16 AND (AU=(MAHDIAN, M? OR MAHDIAN M?))
S19 0 S S16 AND (AU=(SALAVATIPOUR, M? OR SALAVATIPOUR M?))

Higher relevance

d

Subject summary

? t /5,k/all

16/5,K/1 (Item 1 from file: 56) **Links**

Fulltext available through: USPTO Full Text Retrieval Options

Computer and Information Systems Abstracts

0000533040 IP Accession No: 200609-81-107529

Symbolic generation of constrained random logic cells

Costa, R; Curatelli, F; Caviglia, D D; Bisio, G M

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems , v 10 , n 2 , p 220-231 , Feb. 1991

Publication Date: 1991

Publisher: Institute of Electrical and Electronics Engineers, Inc. , 445 Hoes Ln , Piscataway , NJ , 08854-1331

Country Of Publication: USA

Publisher Url: http://ieee.org

Publisher Email: inspec@ieee.org

Document Type: Journal Article

Record Type: Abstract

Language: English

ISSN: 0278-0070

DOI: 10.1109/43.68408

File Segment: Computer & Information Systems Abstracts

Abstract:

A symbolic cell generator (SYC) that can generate the symbolic layout of a generic CMOS logic cell is presented. It accepts as input a SPICE-like netlist describing circuit components, connectivity, and the list of the I/O pins. Using this generator, the user can specify topological constraints on pin and transistor positions, the maximum lengths of polysilicon and diffusion wires, and a preferred layer for each electrical node. Cells are generated according to optimization criteria that take into account not only geometric factors, such as cell area, aspect ratio, and wirelength, but also electrical features, namely capacitance to the substrate and contact and via minimization. The generator's placement strategy includes transistor clustering into regions, global region placement by linear ordering, and two-dimensional local transistor placement. The routing **combines Steiner trees** and Lee algorithms. Object-oriented programming paradigms were used in the implementation of the program, written in C language. Experimental results for small and medium-sized cells are presented

Descriptors: Semiconductor devices; Generators; Transistors; Placement; Optimization; Logic; Constraints; Diffusion layers; Clustering; Capacitance; Integrated circuits; Circuits; Trees; Lists; Object-oriented programming; C (programming language); Criteria; Electric wire; Aspect ratio; Minimization

Subj Catg: 81, Engineering and Sciences

Abstract:

...regions, global region placement by linear ordering, and two-dimensional local transistor placement. The routing **combines Steiner trees** and Lee algorithms. Object-oriented programming paradigms were used in the implementation of the program...

16/5,K/2 (Item 2 from file: 56) **Links**

Fulltext available through: USPTO Full Text Retrieval Options

Computer and Information Systems Abstracts

0000506511 IP Accession No: 200609-81-108011

Near-optimal critical sink routing tree constructions

Boese, K D; Kahng, A B; McCoy, B A; Robins, G

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems , v 14 , n 12 , p 1417-1436 , Dec. 1995

Publication Date: 1995

Publisher: Institute of Electrical and Electronics Engineers, Inc. , 445 Hoes Ln , Piscataway , NJ , 08854-1331

Country Of Publication: USA

Publisher Url: http://ieee.org

Publisher Email: inspec@ieee.org

Document Type: Journal Article

Record Type: Abstract

Language: English

ISSN: 0278-0070

DOI: 10.1109/43.476573

File Segment: Computer & Information Systems Abstracts

Abstract:

We present critical-sink routing tree (CSRT) constructions which exploit available critical-path information to yield high-performance routing trees. Our CS-Steiner and "global slack removal" algorithms **together** modify traditional **Steiner tree** constructions to optimize signal delay at identified critical sinks. We further propose an iterative Elmore routing tree (ERT) construction which optimizes Elmore delay directly, as opposed to heuristically abstracting linear or Elmore delay as in previous approaches. Extensive timing simulations on industry IC and MCM interconnect parameters show that our methods yield trees that significantly improve (by averages of up to 67%) over minimum Steiner routings in terms of delays to identified critical sinks. ERTs also serve as generic high-performance routing trees when no critical sink is specified: for 8-sink nets in standard IC (MCM) technology, we improve average sink delay by 19% (62%) and maximum sink delay by 22% (52%) over the minimum Steiner routing. These approaches provide simple, basic advances over

existing performance-driven routing tree constructions. Our results are complemented by a detailed analysis of the accuracy and fidelity of the Elmore delay approximation; we also exactly assess the suboptimality of our heuristic tree constructions. In achieving the latter result, we develop a new characterization of Elmore-optimal routing trees, as well as a decomposition theorem for optimal Steiner trees, which are of independent interest
Descriptors: Trees; Construction; Delay; Integrated circuits; Construction industry; Heuristic; Accuracy; Time measurements; Optimization; Theorems; Computer simulation; Signal delay; Approximation; Mathematical analysis; Decomposition; Standards; Algorithms; Iterative methods; Computer aided design; Design engineering
Subj Catg: 81, Engineering and Sciences
Abstract:
...information to yield high-performance routing trees. Our CS-Steiner and "global slack removal" algorithms **together** modify traditional **Steiner tree** constructions to optimize signal delay at identified critical sinks. We further propose an iterative Elmore...

16/5,K/3 (Item 3 from file: 56) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
Computer and Information Systems Abstracts

0000263859 IP Accession No: 0170623
General approximation technique for constrained forest problems
Goemans, Michel X; Williamson, David P Massachusetts Inst of Technology, Cambridge, MA, USA
SIAM J COMPUT , v 24 , n 2 , p 296-317 , 1995
Publication Date: 1995
Publisher: SOCIETY FOR INDUSTRIAL AND APPLIED MATHEMATICS , 3600 University City Science Center , Philadelphia , PA , 19104-2688
Country Of Publication: USA
Publisher Url: http://epubs.siam.org
Publisher Email: siam@siam.org
Document Type: Journal Article
Record Type: Abstract
Language: English
ISSN: 0097-5397
File Segment: Computer & Information Systems Abstracts
Abstract:
A general approximation technique for graph-related optimization problems involving an integer program (IP) is proposed. Such graph-related problem is referred to as constraint forest problem. The proposed technique can be applied to problems of covering vertices of graphs with trees, cycles or paths satisfying certain requirements at minimum cost. The algorithm produced from this technique can run in O(n super(2)log n) time and come within a factor of two of optimal for most optimization problems.
Descriptors: Optimization; Graph theory; Algorithms; Trees (mathematics); Combinatorial mathematics; Polynomials; Computational complexity; Integer programming; Set theory; Constraint theory; Linear programming; Functions
Identifiers: Constrained forest problems; Matching; **Steiner tree** problem ; T **joins**; Traveling salesman problem
Subj Catg: C 921.6, Numerical Methods; C 921.5, Optimization Techniques; C 921.4, Combinatorial Mathematics (Includes Graph Theory, Set Theory); C 921.1, Algebra; C 721.1, Computer Theory (Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory)
Identifiers: Constrained forest problems; Matching; **Steiner tree** problem ; T **joins**; Traveling salesman problem

16/5,K/4 (Item 4 from file: 56) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
Computer and Information Systems Abstracts

0000215900 IP Accession No: 2736465
A note on lower bounds for rectilinear Steiner trees.
Salowe, J S Dep. Comp. Sci., Univ. Virginia, Charlottesville, VA 22903, USA
Information Processing Letters , v 42 , n 3 , p 151-152 , 1992
Publication Date: 1992
Publisher: Elsevier Science BV , P.O. Box 211 , Amsterdam , 1000 AE
Country Of Publication: Netherlands
Publisher Url: http://www.elsevier.com
Publisher Email: w.tukker@elsevier.nl
Document Type: Journal Article
Record Type: Citation
Language: English
ISSN: 0020-0190
File Segment: Computer & Information Systems Abstracts
Descriptors: Data structure; **Steiner trees**; Sphere **packing**
Subj Catg: C CS1.8, PROGRAMMING METHODS
Descriptors: Data structure; **Steiner trees**; Sphere **packing**

16/5,K/5 (Item 5 from file: 56) **Links**
Fulltext available through: ScienceDirect

Computer and Information Systems Abstracts

0000139699 IP Accession No: 1893857
Edge-packing of graphs and network reliability.
Colbourn, C J Dep. Comp. Sci., Univ. Auckland, Auckland, New Zealand
DISCRETE MATH. , v 72 , n 1-3 , p 49-61 , 1988
Publication Date: 1988
Conference:
1. Japan Conference of Graph Theory and Applications , Hakone (Japan) , 1-5 June 1986
Document Type: Conference Paper; Journal Article
Record Type: Abstract
Language: English
File Segment: Computer & Information Systems Abstracts
Abstract:
The reliability of a network can be efficiently bounded using graph-theoretical techniques based on edge-packing. We examine the application of combinatorial theorems in edge-packing spanning trees, s, t-paths, and s, t-cuts to the determination of reliability bounds. We compare the resulting bounds with known bounds produced by different techniques, and establish that the edge-packing bounds often produce a substantial improvement. We also establish that three other edge-packing problems arising in reliability bounding are NP-complete, namely edge- **packing** by networks cutsets, **Steiner trees**, and Steiner cutsets.
Descriptors: Networks; Reliability; Graph theory; Np completeness
Identifiers: edge packing
Subj Catg: C CM5.6, GRAPH THEORY
Abstract:
...that three other edge-packing problems arising in reliability bounding are NP-complete, namely edge-**packing** by networks cutsets, **Steiner trees**, and Steiner cutsets.

16/5,K/6 (Item 6 from file: 56) Links
Fulltext available through: ScienceDirect
Computer and Information Systems Abstracts

0000098945 IP Accession No: 1195706
WEAVER: An application of knowledge-based expert systems to detailed routing of VLSI circuits.
Joobbani, R Carnegie-Mellon Univ., Pittsburgh, PA 15213, USA
Addl. Source Info: Dissertation Abstracts International Part B: Science and Engineering [DISS. ABST. INT. PT. B - SCI. & ENG.], vol. 46, no. 5, 1985, 173 pp
Publication Date: 1985
Record Type: Abstract
Language: English
Notes: Order No. FAD DA8513683
File Segment: Computer & Information Systems Abstracts
Abstract:
This thesis presents background about some representative techniques for routing and summarizes their characteristics. It then studies in detail the different factors (such as minimum area, number of vias, wire length, etc.) that affect the routing quality, and the different criteria (such as vertical/horizontal constraint graph, **merging**, minimal rectilinear **Steiner tree**, etc.) that can be used to optimize these factors.
Descriptors: Very large scale integration; Design; Optimization; Computer aided design; Artificial intelligence; Weaver; Microelectronics; Routing; Vlsi (very large scale integration); Expert systems
Identifiers: dissertation
Subj Catg: E ED20.4, HYBRID UNITS; C CA2.1, GENERAL-ARTIFICIAL INTELLIGENCE; C CA19.4, ELECTRONIC DEVICES
Abstract:
...that affect the routing quality, and the different criteria (such as vertical/horizontal constraint graph, **merging**, minimal rectilinear **Steiner tree**, etc.) that can be used to optimize these factors.

16/5,K/7 (Item 1 from file: 35) Links
Dissertation Abs Online

01674575 ORDER NO: AADMQ-31387
OPTIMAL NETWORK DESIGN FOR NATURAL GAS PIPELINES
Author: DOTT, DAWN ROBIN
Degree: M.SC.
Year: 1998
Corporate Source/Institution: UNIVERSITY OF CALGARY (CANADA) (0026)
Adviser: S. C. WIRASINGHE
Source: Volume 37/02 of MASTERS ABSTRACTS. of Dissertations Abstracts International.
PAGE 652 . 117 PAGES
Descriptors: ENGINEERING, CIVIL ; ENGINEERING, PETROLEUM ; ENERGY
Descriptor Codes: 0543; 0765; 0791
ISBN: 0-612-31387-5

Natural gas transportation requires a continuous pipeline network from well-head to burner-tip. This work applies analytical network analysis techniques to the pipeline network design problem. Four issues receive attention: (1) central facility density, (2) spatially-optimal network design, (3) central facility placement, and (4) impact of environment on pipeline design. The first of these problems is solved using a market area model. Here, an appropriate configuration factor for pipeline networks is determined and used to calculate optimal density. Second, concepts of the minimal spanning tree and **Steiner trees** are **combined** in an analytical algorithm for generating near-optimal pipeline networks. Third, a standard optimisation process locates the network median for optimal facility placement. Last, monetary valuation of the environment is shown to have relevance to pipeline projects, and a revealed preference technique is proposed. Case studies of several Alberta pipeline networks illustrate the network concepts presented.

...determined and used to calculate optimal density. Second, concepts of the minimal spanning tree and **Steiner trees** are **combined** in an analytical algorithm for generating near-optimal pipeline networks. Third, a standard optimisation process...

16/5,K/8 (Item 2 from file: 35) **Links**
Dissertation Abs Online

01486513 ORDER NO: AADAA-I9616130
CONSTRAINT-DRIVEN GLOBAL ROUTERS (ANALOG LAYOUT, NETWORKS)
Author: AL-MANSOORI, WAFA A.
Degree: PH.D.
Year: 1996
Corporate Source/Institution: TUFTS UNIVERSITY (0234)
Adviser: KRISHNAMURTHY SOUMYANATH
Source: Volume 5702B of Dissertations Abstracts International.
PAGE 1296 . 114 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0544

In this dissertation we address the signal routing problem for fully differential nets in mixed analog-digital circuits and critical digital nets on integrated circuits. We formally define the fully differential net routing problem as an electrical matching problem. The proposed router is a gridless constraint-driven global router for fully differential terminals which are placed symmetrically about an imaginary axis. Depending on the required circuit performance, two positive parameters $\epsilon\sb{r}$ and $\epsilon\sb{c}$ are used to maintain resistance and capacitance mismatch within acceptable limits. The router matches the net-pair parasitics segment by segment while minimizing a cost function designed for differential signals. The common-mode rejection of crosstalk is included in the cost function and the matching criteria. Using a search technique derived from AI applications (the A* algorithm), both lumped resistance and capacitance are matched. In addition, this technique permits the relaxation of symmetry restriction during the placement phase.

In the case of critical digital nets, a gridless contraint-driven router is proposed. Given a delay bound $t\sb{max}\sb{i}$ for each sink terminal, the router minimizes the combined signal delay to the terminals while simultaneously satisfying each individual delay bound. When compared to minimum **Steiner tree** routers, our router decreased the **combined** delay up to 30%. The maximum signal delay of each net was also improved up to 37% and the net skew was minimized.

...delay to the terminals while simultaneously satisfying each individual delay bound. When compared to minimum **Steiner tree** routers, our router decreased the **combined** delay up to 30%. The maximum signal delay of each net was also improved up...

16/5,K/9 (Item 3 from file: 35) **Links**
Dissertation Abs Online

01350063 ORDER NO: NOT AVAILABLE FROM UNIVERSITY MICROFILMS INT'L.
ON THE DESIGN OF APPROXIMATION ALGORITHMS FOR A CLASS OF GRAPH PROBLEMS (OPTIMIZATION)
Author: WILLIAMSON, DAVID PAUL
Degree: PH.D.
Year: 1993
Corporate Source/Institution: MASSACHUSETTS INSTITUTE OF TECHNOLOGY (0753)
Supervisor: MICHEL X. GOEMANS
Source: Volume 5411B of Dissertations Abstracts International.
PAGE 5787 .
Descriptors: COMPUTER SCIENCE; MATHEMATICS; OPERATIONS RESEARCH
Descriptor Codes: 0984; 0405; 0796

In this thesis, we present a single technique for approximating a large class of graph problems. The technique is based on the standard primal-dual method, and shows the importance of this method in designing approximation algorithms.

The class of problems we consider involves selecting a minimum-cost set of edges such that at least f(S) edges have exactly one endpoint in each subset of vertices S, for certain easily characterized functions f. We show that our technique leads to $2{\cal H}(f\sb{\rm max})$-approximation algorithms for problems in this class, where $f\sb{\rm max} = max\sb{s} f(S)$ and ${\cal H}(k)$ is the harmonic function $1 + {1\over2} + \... + {1\over k}.$ The class captures a wide variety of classical and complex problems in combinatorial optimization, including the minimum-cost spanning tree, Steiner tree, generalized **Steiner tree**, survivable network design, T-**join**, minimum-weight perfect matching (under triangle inequality), two-matching (under triangle inequality), and location-design problems. Our algorithm runs in $O(n\sp2m\sp\prime f\sb{\rm max} + n\sp2\omega\sb{f}f\sb{\rm max})$ time on a graph of n vertices and m edges, where $m\sp\prime$ = min($nf\sb{\rm max}, m)$ and $\omega\sb{f}$ is the time to compute the function f. We obtain faster time bounds for specific problems of interest.

The algorithms produced first generalize classical algorithms for minimum-cost spanning trees and shortest paths. Second, they provide approximation algorithms for problems in P (such as the minimum-weight perfect matching problem under triangle inequality) that run asymptotically faster than the best-known algorithms that solve these problems exactly. Third, they provide approximation algorithms for problems which had no previously known approximation algorithm. For instance, the technique gives the first approximation algorithm for the survivable network design problem, which is the problem of finding a minimum-cost set of edges such that there are $r\sb{ij}$ edge-disjoint paths between each pair of vertices i and j. Fourth, the algorithms given by the technique improve on the running time and/or the approximation factor of several known approximation algorithms.

Extensions of the main technique of this thesis lead to approximation algorithms for problems which do not fall in the class of problems mentioned above. For example, we give a 2-approximation algorithm for the prize-collecting traveling salesman problem and a $2{\cal H}(k)$- approximation algorithm for the minimum-cost k-vertex-connected subgraph problem.

Finally, we conduct an experimental study of our 2-approximation algorithm for minimum-weight perfect matching on Euclidean instances. We present computational results for both random and real-world instances having between 1,000 and 131,072 vertices. The results indicate that our algorithm generates a matching within 2% of optimality in most cases. In over 1,400 experiments, the algorithm was never more than 4% from optimal. (Copies available exclusively from MIT Libraries, Rm. 14-0551, Cambridge, MA 02139-4307. Ph. 617-253-5668; Fax 617-253-1690.) (Abstract shortened by UMI.)

...and complex problems in combinatorial optimization, including the minimum-cost spanning tree, Steiner tree, generalized **Steiner tree**, survivable network design, T-**join**, minimum-weight perfect matching (under triangle inequality), two-matching (under triangle inequality), and location-design...

16/5,K/10 (Item 4 from file: 35) **Links**
Dissertation Abs Online

887218 ORDER NO: AAD85-13683
WEAVER: AN APPLICATION OF KNOWLEDGE-BASED EXPERT SYSTEMS TO DETAILED ROUTING OF VLSI CIRCUITS (DESIGN, ROUTING)
Author: JOOBBANI, ROSTAM
Degree: PH.D.
Year: 1985
Corporate Source/Institution: CARNEGIE-MELLON UNIVERSITY (0041)
Source: Volume 4605B of Dissertations Abstracts International.
PAGE 1617 . 173 PAGES
Descriptors: COMPUTER SCIENCE
Descriptor Codes: 0984

Routing of VLSI chips is an important, time consuming, and difficult problem. The difficulty of the problem is attributed to the large number of often conflicting factors that affect the routing quality. Traditional techniques have approached routing by ignoring some of these factors and imposing unnecessary constraints in order to make routing tractable. In addition to the imposition of these restrictions, which simplify the problems to a degree but at the same time reduce the routing quality, traditional approaches use brute force. They often transform the problem into mathematical or graph problems and completely ignore the specific knowledge about the routing task that can greatly help the solution.

This thesis overcomes some of the above problems and presents a system that performs routing close to what human designers do. In other words it heavily capitalizes on the knowledge of human expertise in this area, it does not impose unnecessary constraints, it considers all the different factors that affect the routing quality, and most importantly it allows constant user interaction throughout the routing process.

To achieve the above, this thesis presents background about some representative techniques for routing and summarizes their characteristics. It then studies in detail the different factors (such as minimum area, number of vias, wire length, etc.) that affect the routing quality, and the different criteria (such as vertical/horizontal constraint graph, **merging**, minimal rectilinear **Steiner tree**, etc.) that can be used to optimize these factors.

The result of the above study is then used to implement WEAVER, a knowledge-based routing expert. To evaluate the effectiveness of the approach, a number of experiments are performed which compare WEAVER's performance with the traditional approaches. These experiments show: a dramatic improvement over the traditional approaches; a performance equal to or better than human expertise; the effectiveness of the use of human knowledge; and the viability of the technique of knowledge-based expert systems in the routing domain, the foundation on which WEAVER is based.

...that affect the routing quality, and the different criteria (such as vertical/horizontal constraint graph, **merging**, minimal rectilinear **Steiner tree**, etc.) that can be used to optimize these factors.

The result of the above study...

16/5,K/11 (Item 1 from file: 8) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
Ei Compendex(R)

09129097 **E.I. No:** EIP02377082143
Title: Routing strategies for multicast packet radio networks
Author: Hemminger, Thomas L.; Coulston, Chris; Pomalaza-Raez, Carlos A.
Corporate Source: Sch. of Eng. and Eng. Technology Penn State University Behrend College, Erie, PA 16563, United States
Source: International Journal of Smart Engineering System Design v 4 n 3 July/September 2002. p 215-223

Publication Year: 2002
CODEN: IJSDFJ **ISSN:** 1025-5818
Language: English
Document Type: JA; (Journal Article) **Treatment:** T; (Theoretical)
Journal Announcement: 0209W3
Abstract: A common problem in a packet radio network (PRN) environment is to construct a multicasting network from a single source to a set of remote destinations which minimizes the number of transmissions. This problem is known to be NP-complete, thus computing an optimal solution may be infeasible for sizable networks. This paper provides two alternative solutions to this problem. The first is a heuristic algorithm which iteratively builds a spanning tree from the destinations to the source. A second solution, included for comparative purposes, is based on the Hopfield neural network whose dynamics are governed by a motion equation and a set of constraints. Both solutions are tested on a variety of instances against an optimal algorithm. Results show the approaches form good solutions (the number of transmissions is within about 3% of the optimum) and run in a fraction of the time required to form the optimal solution. 22 Refs.
Descriptors: *Packet networks; Multicasting; Routers; Optimization; Heuristic methods; Iterative methods; Neural networks; Constraint theory; Problem solving; Algorithms
Identifiers: Multicast **packet** radio networks (PRN); **Steiner** minimal **tree** (SMT) problems
Classification Codes:
721.1 (Computer Theory (Includes Formal Logic, Automata Theory, Switching Theory & Programming Theory)); 722.3 (Data Communication, Equipment & Techniques); 921.5 (Optimization Techniques); 921.6 (Numerical Methods); 723.4 (Artificial Intelligence)
721 (Computer Circuits & Logic Elements); 716 (Electronic Equipment, Radar, Radio & Television); 717 (Electro-Optical Communication); 718 (Telephone & Other Line Communications); 722 (Computer Hardware); 921 (Applied Mathematics); 723 (Computer Software, Data Handling & Applications)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATION ENGINEERING); 92 (ENGINEERING MATHEMATICS)
Identifiers: Multicast **packet** radio networks (PRN); **Steiner** minimal **tree** (SMT) problems

16/5,K/12 (Item 2 from file: 8) **Links**
Fulltext available through: ScienceDirect
Ei Compendex(R)

09127004 **E.I. No:** EIP02377076628
Title: Effective location-guided tree construction algorithms for small group multicast in MANET
Author: Chen, Kai; Nahrstedt, Klara
Corporate Source: Computer Science Department Univ. Illinois at Urbana-Champaign, Urbana, IL 61801, United States
Conference Title: IEEE Infocom 2002
Conference Location: New York, NY, United States **Conference Date:** 20020623-20020627
Sponsor: IEEE
E.I. Conference No.: 59460
Source: Proceedings - IEEE INFOCOM v 3 2002. p 1180-1189 (IEEE cat n 02ch37364)
Publication Year: 2002
CODEN: PINFEZ **ISSN:** 0743-166X
Language: English
Document Type: CA; (Conference Article) **Treatment:** A; (Applications); T; (Theoretical)
Journal Announcement: 0209W3
Abstract: Group communication has become increasingly important in mobile ad hoc networks (MANET). Current multicast routing protocols in MANET have been shown to have large overhead due to dynamic network topology. To overcome this problem, there is a recent shift towards stateless multicast in small groups (DDM left bracket 1 right bracket). DDM queries the underlying unicast routing protocol to forward data packets towards members of a multicast group. The multicast distribution tree in DDM is implicit and cannot be controlled by the upper transport and application layers. In this paper, we introduce another small group multicast scheme, based on packet encapsulation, which uses novel packet distribution tree construction algorithms for efficient data delivery. The packet distribution tree is constructed explicitly with the goal of minimizing the overall bandwidth cost of the tree. The tree construction algorithms include a location-guided k-ary (LGK) tree and a location-guided Steiner (LGS) tree. Both of them utilize the geometric locations of the destination nodes as heuristics to compute the trees, and are accompanied by a hybrid location update mechanism to disseminate location information among a group of nodes. Our simulation results show that LGS tree has lower bandwidth cost than LGK tree when the location information of the nodes is up-to-date, and its cost is similar to that of an optimal Steiner multicast tree. When location information of the nodes is out-dated, LGK tree outperforms LGS tree due to its lower computational complexity. 24 Refs.
Descriptors: *Multicasting; Mobile telecommunication systems; Information dissemination; Algorithms; Trees (mathematics); Network protocols; Packet switching; Geometry; Heuristic methods; Computer simulation; Computational complexity; Optimization
Identifiers: Mobile ad hoc networks; Group communication; Tree construction algorithm; Location update mechanism; **Steiner tree**; **Packet** encapsulation; **Packet** distribution tree
Classification Codes:
716.1 (Information & Communication Theory); 716.3 (Radio Systems & Equipment); 903.2 (Information Dissemination); 723.1 (Computer Programming); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory); 723.5 (Computer Applications)
716 (Electronic Equipment, Radar, Radio & Television); 903 (Information Science); 723 (Computer Software, Data Handling & Applications); 921 (Applied Mathematics)

71 (ELECTRONICS & COMMUNICATION ENGINEERING); 90 (ENGINEERING, GENERAL); 72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)
Identifiers: Mobile ad hoc networks; Group communication; Tree construction algorithm; Location update mechanism; **Steiner tree**; **Packet** encapsulation; **Packet** distribution tree

16/5,K/13 (Item 3 from file: 8) **Links**
Fulltext available through: ScienceDirect
Ei Compendex(R)

09087731 **E.I. No:** EIP02287010887
Title: A genetic approach to analog module placement with simulated annealing
Author: Zhang, Lihong; Kleine, Ulrich
Corporate Source: Institute for Electronics Signal Processing and Commun. (IESK) Otto-von-Guericke Univ. of Magdeburg, D-39016 Magdeburg, Germany
Conference Title: 2002 IEEE International Symposium on Circuits and Systems
Conference Location: Phoenix, AZ, United States **Conference Date:** 20020526-20020529
Sponsor: IEEE
E.I. Conference No.: 59247
Source: Proceedings - IEEE International Symposium on Circuits and Systems v 1 2002. p I/345-I/348 (IEEE cat n 02ch37353)
Publication Year: 2002
CODEN: PICSDI **ISSN:** 0271-4310
Language: English
Document Type: CA; (Conference Article) **Treatment:** T; (Theoretical); X; (Experimental)
Journal Announcement: 0207W2
Abstract: This paper presents a novel approach to analog module placement with the combination of genetic algorithm and simulated annealing. The approach is based on the bottom-left relative placement represented by binary tree. It is superior to the other three approaches which were implemented with pure simulated annealing or genetic algorithms. A fractional factorial experiment was conducted using an orthogonal array to study the algorithm parameters. A meta-GA was applied to determine the exact parameter values. The dedicated cost function covers the special requirements of analog integrated circuits. The experimental results show this promising algorithm makes the best performance with the least mean cost and standard deviation over all the other compared approaches. 12 Refs.
Descriptors: *Integrated circuit layout; Linear integrated circuits; Computer aided design; Genetic algorithms; Simulated annealing; Trees (mathematics); Parameter estimation; Heuristic methods; MOS devices; Computer simulation
Identifiers: Analog module placement; Analog integrated circuits; Bottom left relative placement; Software **package** ALADIN; Binary tree; **Steiner tree** problem; Cost function
Classification Codes:
714.2 (Semiconductor Devices & Integrated Circuits); 723.5 (Computer Applications); 723.1 (Computer Programming); 921.5 (Optimization Techniques); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory); 921.6 (Numerical Methods)
714 (Electronic Components & Tubes); 723 (Computer Software, Data Handling & Applications); 921 (Applied Mathematics)
71 (ELECTRONICS & COMMUNICATION ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)
Identifiers: Analog module placement; Analog integrated circuits; Bottom left relative placement; Software **package** ALADIN; Binary tree; **Steiner tree** problem; Cost function

16/5,K/14 (Item 4 from file: 8) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
Ei Compendex(R)

09017838 **E.I. No:** EIP02116883543
Title: Buffered Steiner trees for difficult instances
Author: Sullivan, A.J.; Alpert, Charles J.; Gandham, Gopal; Hrkic, Milos; Hu, Jiang ; Kahng, Andrew B.; Lillis, John; Liu, Bao; Quay, Stephen T.; Sapatnekar, Sachin S.
Corporate Source: IBM Corporation, Austin, TX 78758, United States
Source: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems v 21 n 1 January 2002. p 3-14
Publication Year: 2002
CODEN: ITCSDI **ISSN:** 0278-0070
Language: English
Document Type: JA; (Journal Article) **Treatment:** T; (Theoretical)
Journal Announcement: 0203W3
Abstract: With the rapid scaling of integrated-circuit technology, buffer insertion has become an increasingly critical optimization technique in high-performance design. The problem of finding a buffered Steiner tree with optimal delay characteristics has been an active area of research and excellent solutions exist for most instances. However, there exists a class of real "difficult" instances, which are characterized by a large number of sinks (e.g., 20-100), large variations in sink criticalities, nonuniform sink distribution, and varying polarity requirements. Existing techniques are either inefficient, wasteful of buffering resources, or unable to find a high-quality solution. We propose C-tree, a two-level construction that first clusters sinks with common characteristics **together**, constructs low-level **Steiner trees** for each cluster, then performs a timing-driven Steiner construction on the top-level clustering. We show that this hierarchical approach can

achieve higher quality solutions with fewer resources compared to traditional timing-driven Steiner trees. 23 Refs.
Descriptors: *Integrated circuit layout; Trees (mathematics); Electric network topology; Interconnection networks; Optimization
Identifiers: Buffered Steiner trees
Classification Codes:
714.2 (Semiconductor Devices & Integrated Circuits); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory); 703.1 (Electric Networks); 921.5 (Optimization Techniques)
714 (Electronic Components & Tubes); 921 (Applied Mathematics); 703 (Electric Circuits); 721 (Computer Circuits & Logic Elements)
71 (ELECTRONICS & COMMUNICATION ENGINEERING); 92 (ENGINEERING MATHEMATICS); 70 (ELECTRICAL ENGINEERING, GENERAL); 72 (COMPUTERS & DATA PROCESSING)
Abstract: ...We propose C-tree, a two-level construction that first clusters sinks with common characteristics **together**, constructs low-level **Steiner trees** for each cluster, then performs a timing-driven Steiner construction on the top-level clustering...

16/5,K/15 (Item 5 from file: 8) **Links**
Fulltext available through: ScienceDirect
Ei Compendex(R)

08933797 **E.I. No:** EIP01456717510
Title: Efficient algorithms for the multicast trees under the packet-replication restrictions
Author: Chung, S.-J.; Hong, S.-P.; Chung, H.-S.
Corporate Source: Seoul National University, Seoul, South Korea
Source: IEICE Transactions on Communications v E84-B n 9 September 2001. p 2670-2680
Publication Year: 2001
CODEN: ITRCEC **ISSN:** 0916-8516
Language: English
Document Type: JA; (Journal Article) **Treatment:** A; (Applications); T; (Theoretical)
Journal Announcement: 0111W2
Abstract: In this paper, we are concerned in obtaining multicast trees in packet-switched networks such as ATM nets, when there exist constraints on the packet (cell)-replication capabilities of the individual switching nodes. This problem can be formulated as the Steiner tree problem with degree bounds on the nodes, so we call it the Degree-Constrained Steiner Tree problem (DCST). Four heuristic algorithms are proposed: the first is a **combined** version of two well-known **Steiner tree** algorithms, heuristic Naive and the shortest path heuristic (SPH), and the second is a relaxation algorithm based on a mathematical formulation of the DCST, and the last two use a tree reconfiguration scheme based on the concept of 'logical link.' We experimentally compare our algorithms with the previous ones in three respects; number of solved instances, objective value or tree cost, and computation time. The experimental results show that there are few instances unsolved by our algorithms, and the objective values are mostly within 5% of optimal. Computation times are also acceptable. 30 Refs.
Descriptors: *Multicasting; Algorithms; Packet networks; Constraint theory; Heuristic methods; Trees (mathematics); Problem solving
Identifiers: Multicast trees; Packet-replication restrictions; Relaxation algorithm
Classification Codes:
716.1 (Information & Communication Theory); 723.5 (Computer Applications); 721.1 (Computer Theory (Includes Formal Logic, Automata Theory, Switching Theory & Programming Theory)); 921.6 (Numerical Methods)
716 (Electronic Equipment, Radar, Radio & Television); 723 (Computer Software, Data Handling & Applications); 721 (Computer Circuits & Logic Elements); 921 (Applied Mathematics)
71 (ELECTRONICS & COMMUNICATION ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)
Abstract: ...Degree-Constrained Steiner Tree problem (DCST). Four heuristic algorithms are proposed: the first is a **combined** version of two well-known **Steiner tree** algorithms, heuristic Naive and the shortest path heuristic (SPH), and the second is a relaxation...

16/5,K/16 (Item 6 from file: 8) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
Ei Compendex(R)

08516143 **E.I. No:** EIP00035102781
Title: Associative-skew clock routing problem
Author: Chen, Yu; Kahng, Andrew B.; Qu, Gang; Zelikovsky, Alexander
Corporate Source: UCLA, Los Angeles, CA, USA
Conference Title: Proceedings of the 1999 IEEE/ACM International Conference on Computer-Aided Design (ICCAD-99)
Conference Location: San Jose, CA, USA **Conference Date:** 19991107-19991111
E.I. Conference No.: 56397
Source: IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers 1999. p 168-172
Publication Year: 1999
CODEN: DICDFD **ISSN:** 1092-3152
Language: English
Document Type: JA; (Journal Article) **Treatment:** A; (Applications); T; (Theoretical)
Journal Announcement: 0005W3

Abstract: We introduce the associative skew clock routing problem, which seeks a clock routing tree such that zero skew is preserved only within identified groups of sinks. The associative skew problem is easier to address within current EDA frameworks than useful-skew (skew-scheduling) approaches. and defines an interesting tradeoff between the traditional zero-skew clock routing problem (one sink group) and the Steiner minimum tree problem (n sink groups). We present a set of heuristic building blocks, including an efficient and optimal method of merging two zero-skew trees such that zero skew is preserved within the sink sets of each tree. Finally, we list a number open issues for research and practical application. (Author abstract) 21 Refs.
Descriptors: *Routers; Trees (mathematics); Set theory; Heuristic programming; Computer aided design; VLSI circuits; Topology; Algorithms
Identifiers: Associative skew clock routing; Rectilinear **Steiner** minimum **tree**; Zero skew tree; Deferred **merge** embedding; Bounded skew tree
Classification Codes:
722.3 (Data Communication, Equipment & Techniques); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory); 723.1 (Computer Programming); 723.5 (Computer Applications); 714.2 (Semiconductor Devices & Integrated Circuits)
722 (Computer Hardware); 921 (Applied Mathematics); 723 (Computer Software); 714 (Electronic Components)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS); 71 (ELECTRONICS & COMMUNICATIONS)
Identifiers: Associative skew clock routing; Rectilinear **Steiner** minimum **tree**; Zero skew tree; Deferred **merge** embedding; Bounded skew tree

16/5,K/17 (Item 7 from file: 8) **Links**
Fulltext available through: ScienceDirect
Ei Compendex(R)

07868331 **E.I. No:** EIP97113926477
Title: DMRP: A distributed multicast routing protocol for ATM networks
Author: Venkateswaran, R.; Raghavendra, C.S.; Chen, X.; Kumar, V.P.
Corporate Source: Washington State Univ, Pullman, WA, USA
Conference Title: Proceedings of the 1997 IEEE ATM Workshop
Conference Location: Lisboa, Portugal **Conference Date:** 19970525-19970528
Sponsor: IEEE
E.I. Conference No.: 47249
Source: IEEE ATM Workshop, Proceedings 1997. IEEE, Piscataway, NJ, USA. p 263-271
Publication Year: 1997
CODEN: 002708
Language: English
Document Type: CA; (Conference Article) **Treatment:** A; (Applications); G; (General Review)
Journal Announcement: 9801W1
Abstract: In this paper, we present a Distributed Multicast Routing Protocol (DMRP) for dynamic computation of multicast trees. This protocol is a distributed version of a centralized heuristic for dynamic Steiner Tree computation. The protocol is deadlock-free and is a correct implementation of the centralized heuristic. It can be easily extended to the hierarchical framework supported by ATM Forum's PNNI protocols. This makes the protocol very scalable. Our motivation is to make this protocol a standard for multicasting under the PNNI framework. Our protocol draws a lot of inspiration from PIM, which has been proposed as the standard for multicasting in the internet domain. We would like to emphasize that unlike PIM which caters to maintaining only soft-states, DMRP maintains hard states. The hard states are required under the ATM framework and make the DMRP protocol compatible with the philosophy of PNNI. The sharing of the multicast tree among multiple senders makes effective use of the network resources. This reduces the overall cost of the multicast tree. The protocol relies on Participant Initiated Join, where the participant who wants to establish connection with the multicast group computes the path to the already existing multicast tree. Using simulations, we show that the number of messages generated before a participant can join the multicast tree is small. Further, the join latency is also small. The simplicity of the protocol lends itself to easy implementation for the support of multipoint connections under the PNNI framework. (Author abstract) 6 Refs.
Descriptors: *Asynchronous transfer mode; Network protocols; Congestion control (communication); Heuristic methods; Computer simulation; Trees (mathematics)
Identifiers: Distributed multicasting routing protocols (DMRP); **Steiner Tree** computation; Participant initiated **join**
Classification Codes:
723.5 (Computer Applications); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory)
716 (Radar, Radio & TV Electronic Equipment); 723 (Computer Software) ; 921 (Applied Mathematics)
71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)
Identifiers: Distributed multicasting routing protocols (DMRP); **Steiner Tree** computation; Participant initiated **join**

16/5,K/18 (Item 8 from file: 8) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
Ei Compendex(R)

07800346 **E.I. No:** EIP97083784406
Title: Packing Steiner trees: Separation algorithms
Author: Grotschel, M.; Martin, A.; Weismantel, R.

Corporate Source: Konrad-Zuse-Zentrum fur Informationstechnik Berlin, Heilbronner Strasse 10, 10711 Berlin, Germany
Source: SIAM Journal on Discrete Mathematics v 9 n 2 1996. p 233-257
Publication Year: 1996
CODEN: SJDMEC **ISSN:** 0895-4801
Language: English
Document Type: JA; (Journal Article)
Journal Announcement: 9710W4
Abstract: In this paper, we investigate separation problems for classes of inequalities valid for the polytope associated with the **Steiner tree packing** problem, a problem that arises, e.g., in very large-scale integration (VLSI) routing. The separation problem for Steiner partition inequalities is NP-hard in general. We show that it can be solved in polynomial time for those instances that come up in switchbox routing. Our algorithm uses dynamic programming techniques. These techniques are also applied to the much more complicated separation problem for alternating cycle inequalities. In this case, we can compute in polynomial time, given some point y, a lower bound for the gap x- a**T y over all alternating cycle inequalities a**T x greater than equivalent to alpha . This gives rise to a very effective separation heuristic. A by-product of our algorithm is the solution of a combinatorial optimization problem that is interesting in its own right: find a shortest path in a graph where the 'length' of a path is its usual length minus the length of its longest edge. 16 Ref.
Descriptors: *Algorithms; Dynamic programming
Identifiers: Polynomial time; Polytope; Steiner system; Graph path; Shortest path; Combinatorial optimization
Classification Codes:
921.5 (Optimization Techniques)
921 (Applied Mathematics)
92 (ENGINEERING MATHEMATICS)
Title: Packing Steiner trees: Separation algorithms
Abstract: ...we investigate separation problems for classes of inequalities valid for the polytope associated with the Steiner tree packing problem, a problem that arises, e.g., in very large-scale integration (VLSI) routing. The...

16/5,K/19 (Item 9 from file: 8) Links
Fulltext available through: SpringerLink USPTO Full Text Retrieval Options
Ei Compendex(R)

07782101 **E.I. No:** EIP97083783920
Title: Steiner tree packing problem in VLSI design
Author: Groetschel, M.; Martin, A.; Weismantel, R.
Corporate Source: Konrad-Zuse-Zentrum fuer Informationstechnik Berlin, Berlin, Ger
Source: Mathematical Programming, Series B v 78 n 2 Aug 1 1997. p 265-281
Publication Year: 1997
CODEN: MPSBEU **ISSN:** 0025-5610
Language: English
Document Type: JA; (Journal Article) **Treatment:** T; (Theoretical); X; (Experimental)
Journal Announcement: 9710W1
Abstract: In this paper we describe several versions of the routing problem arising in VLSI design and indicate how the **Steiner tree packing** problem can be used to model these problems mathematically. We focus on switchbox muting problems and provide integer programming formulations for routing in the knock-knee and in the Manhattan model. We give a brief sketch of cutting plane algorithms that we developed and implemented for these two models. We report on computational experiments using standard test instances. Our codes are able to determine optimum solutions in most cases, and in particular, we can show that some of the instances have no feasible solution if Manhattan routing is used instead of knock-knee routing. (Author abstract) 20 Refs.
Descriptors: *Integer programming; VLSI circuits; Integrated circuit layout; Trees (mathematics); Mathematical models
Identifiers: Steiner tree packing; Switchbox routing; Manhattan model
Classification Codes:
921.5 (Optimization Techniques); 714.2 (Semiconductor Devices & Integrated Circuits); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory)
921 (Applied Mathematics); 714 (Electronic Components)
92 (ENGINEERING MATHEMATICS); 71 (ELECTRONICS & COMMUNICATIONS)
Title: Steiner tree packing problem in VLSI design
Abstract: ...describe several versions of the routing problem arising in VLSI design and indicate how the Steiner tree packing problem can be used to model these problems mathematically. We focus on switchbox muting problems...
Identifiers: Steiner tree packing; Switchbox routing; Manhattan model

16/5,K/20 (Item 10 from file: 8) Links
Fulltext available through: ScienceDirect
Ei Compendex(R)

07364610 **E.I. No:** EIP96033109454
Title: Minimum-cost node-disjoint Steiner trees in series-parallel networks
Author: Chopra, Sunil; Talluri, Kalyan T.
Corporate Source: Northwestern Univ, Evanston, IL, USA
Source: VLSI Design v 4 n 1 1996. p 53-57
Publication Year: 1996

CODEN: VLDEEZ
Language: English
Document Type: JA; (Journal Article) **Treatment:** T; (Theoretical)
Journal Announcement: 9605W3
Abstract: The routing problem in VLSI-layout can be modeled as a problem of **packing** node-disjoint **Steiner trees** in a graph. The problem is as follows: Given an undirected network G equals (V,E) and a net list Psi equals left brace N//i, i equals 1,..., r right brace , a family Gamma //G equals left brace T//N//(//i//) equals (V//N//(//i//), E//N//(//i//)), i equals 1,..., r right brace is a node-disjoint family of Steiner trees spanning Psi if T//N//(//i//) is a Steiner tree spanning N//i for i equals 1,..., r and V//N//(//i//) qq V//N//(//j//) equals for i does not equal j. The edge-disjoint version of this problem is known to be NP-hard for series-parallel graphs (see Richey and Parker left bracket 5 right bracket). In this paper we give a O(n**5) algorithm for finding a minimum-cost node-disjoint family of Steiner trees in series-parallel networks. Our algorithm can be extended to k-trees and is polynomial for fixed k. (Author abstract) 6 Refs.
Descriptors: *Integrated circuit layout; Trees (mathematics); Mathematical models; Computational complexity; Algorithms; Polynomials
Identifiers: Steiner trees; Series parallel graphs; Routing problem
Classification Codes:
714.2 (Semiconductor Devices & Integrated Circuits); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory); 921.1 (Algebra)
714 (Electronic Components); 921 (Applied Mathematics); 721 (Computer Circuits & Logic Elements)
71 (ELECTRONICS & COMMUNICATIONS); 92 (ENGINEERING MATHEMATICS); 72 (COMPUTERS & DATA PROCESSING)
Abstract: The routing problem in VLSI-layout can be modeled as a problem of **packing** node-disjoint **Steiner trees** in a graph. The problem is as follows: Given an undirected network G equals (V...

16/5,K/21 (Item 11 from file: 8) Links
Fulltext available through: ScienceDirect
Ei Compendex(R)

05905255 **E.I. Monthly No:** EIM9005-021516
Title: Automatic generation of symbolic cells from a net-list description.
Author: Costa, Raffaele; Curatelli, Francesco; Caviglia, Daniele D.; Bisio, Giacomo M.
Corporate Source: DIBE, Univ of Genova, Genoa, Italy
Conference Title: COMPEURO '89 - 3rd Annual European Computer Conference
Conference Location: Hamburg, West Ger **Conference Date:** 19890508
Sponsor: IEEE, Computer Soc, Los Alamitos, CA, USA; Gesellschaft fuer Informatik, West Ger; Verband Deutscher Elektrotechniker, Frankfurt am Main, West Ger
E.I. Conference No.: 12818
Source: VLSI and Computer Peripherals. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. Available from IEEE Service Cent (cat n 89CH2704-5), Piscataway, NJ, USA. p 5/35-39
Publication Year: 1989
ISBN: 0-8186-1940-6
Language: English
Document Type: PA; (Conference Paper) **Treatment:** A; (Applications)
Journal Announcement: 9005
Abstract: A tool capable of synthesizing the symbolic layout of a CMOS cell from its circuit descriptions is presented. The synthesis process is guided by topological constraints on pin and transistor positions, maximum lengths of poly and diffusion wires, and the specification of a preferred layer for each electrical node. The optimization criteria take into account cell area and aspect ratio, wire length, capacitance to the substrate, and contact and via minimization. The novel placement strategy includes transistor clustering into regions, global region placement by linear ordering, and two-dimensional local transistor placement. The routing **combines Steiner trees** and Lee algorithms. The program is fast and has been thoroughly tested on small and medium-sized cells. 13 Refs.
Descriptors: *INTEGRATED CIRCUITS, VLSI--*Layout; SEMICONDUCTOR DEVICES, MOS; TRANSISTORS; COMPUTER PROGRAMMING--Algorithms
Identifiers: CMOS CELLS; NETLIST DISPLAYS; STEINER TREES; LEE ALGORITHMS
Classification Codes:
713 (Electronic Circuits); 714 (Electronic Components); 723 (Computer Software)
71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)
Abstract: ...regions, global region placement by linear ordering, and two-dimensional local transistor placement. The routing **combines Steiner trees** and Lee algorithms. The program is fast and has been thoroughly tested on small and...

16/5,K/22 (Item 1 from file: 65) Links
Fulltext available through: ScienceDirect
Inside Conferences

01224966 **Inside Conference Item ID:** CN012026110
Two Steiner Tree Packing Problems
Pulleyblank, W. R.
Conference: Theory of computing - 27th Annual symposium
ANNUAL ACM SYMPOSIUM ON THEORY OF COMPUTING , 1995; VOL 27 P: 383-387

ACM Press, 1995
ISSN: 0737-8017 **ISBN:** 0897917189
Language: English **Document Type:** Conference Papers
Sponsor: Association for Computing Machinery
Location: Las Vegas, NV
Date: May 1995 (199505) (199505)
British Library Item Location: 1073.870000
Descriptors: computing; ACM
Two Steiner Tree Packing Problems

16/5,K/23 (Item 2 from file: 65) **Links**
Fulltext available through: ScienceDirect
Inside Conferences

00737620 **Inside Conference Item ID:** CN007195930
Steiner Trees and Packing Constants in Graph-Metric Spaces
Prass, P.
Conference: Graphs and combinatorial optimization - 3rd Workshop
PB REPORTS , PB94-110947 P: 24-26
[np], [nd]
Language: English **Document Type:** Conference Papers and programme
Sponsor: United States Department of Commerce
Location: Enschede, The Netherlands
Date: Jun 1993 (199306) (199306)
British Library Item Location: 6413.350000F
Note:
3; microfiche
Descriptors: graphs; combinatorial optimization; USDOC
Steiner Trees and Packing Constants in Graph-Metric Spaces

16/5,K/24 (Item 1 from file: 2) **Links**
Fulltext available through: John Wiley and Sons USPTO Full Text Retrieval Options
INSPEC

08430399 **INSPEC Abstract Number:** B2002-12-2570A-018
Title: A branch-and-price algorithm for switch-box routing
Author Jorgensen, D.G.; Meyling, M.
Author Affiliation: Dept. of Comput. Sci., Copenhagen Univ., Denmark
Journal: Networks vol.40, no.1 p. 13-26
Publisher: Wiley ,
Publication Date: Aug. 2002 **Country of Publication:** USA
CODEN: NTWKAA **ISSN:** 0028-3045
SICI: 0028-3045(200208)40:1L.13:BPAS;1-X
Material Identity Number: N073-2002-005
Item Identifier (DOI): 10.1002/net.10029
Language: English **Document Type:** Journal Paper (JP)
Treatment: Practical (P); Theoretical (T)
Abstract: Routing in VLSI design concerns the wiring of a chip after the logical modules have been placed. A subproblem occurring in VLSI design is switch-box routing. Switch-box routing can be formulated as the problem of **packing Steiner trees** in a grid graph. The only previous exact solution method for switch-box routing uses a branch-and-cut approach. The aim of this work is to solve the switch-box routing problem to optimality by using a branch-and-price algorithm based on an IP model where variables represent Steiner trees and where the pricing problem becomes the problem of finding a Steiner tree in a graph. In the primal algorithm, the focal points are branching strategy, pricing strategy, perturbation of the linear program, and computation of lower bounds to terminate column generation early. The final implementation yields optimal solutions in the knock-knee model to seven classic switch-box instances, of which three had not been solved to optimality prior to this work. (18 Refs)
Subfile: B
Descriptors: integrated circuit layout; network routing; optimisation; trees (mathematics); VLSI
Identifiers: branch-and-price algorithm; switch-box routing; VLSI design; chip wiring; Steiner trees; grid graph; branching strategy; pricing strategy; linear program perturbation; column generation termination; knock-knee model; optimization
Class Codes: B2570A (Semiconductor integrated circuit design, layout, modelling and testing); B0250 (Combinatorial mathematics); B1110 (Network topology)

Abstract: ...design is switch-box routing. Switch-box routing can be formulated as the problem of **packing Steiner trees** in a grid graph. The only previous exact solution method for switch-box routing uses...

16/5,K/25 (Item 2 from file: 2) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
INSPEC

08185265 **INSPEC Abstract Number:** B2002-03-0260-059, C2002-03-1180-071
Title: A branch-and-price algorithm for the Steiner tree packing problem
Author Gue-woong Jeong; Kyungsik Lee; Sungsoo Park; Kyungchul Park
Author Affiliation: Dept. of Ind. Eng., Korea Adv. Inst. of Sci. & Technol., Seoul, South Korea
Journal: Computers & Operations Research vol.29, no.3 p. 221-41
Publisher: Elsevier ,
Publication Date: March 2002 **Country of Publication:** UK
CODEN: CMORAP **ISSN:** 0305-0548
SICI: 0305-0548(200203)29:3L.221:BPAS;1-0
Material Identity Number: C175-2002-002
U.S. Copyright Clearance Center Code: 0305-0548/02/$20.00
Document Number: S0305-0548(00)00066-6
Language: English **Document Type:** Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: The paper, deals with the **Steiner tree packing** problem. For a given undirected graph G=(V,E) with positive integer capacities and nonnegative weights on its edges, and a list of node sets (nets), the problem is to find a connection of nets which satisfies the edge capacity limits and minimizes the total weights. We focus on the switchbox routing problem in knock-knee model and formulate this problem as an integer programming problem using Steiner tree variables. We-develop a branch-and-price algorithm. The algorithm is applied on some standard test instances and we compare the performances with the results using a cutting plane approach. Computational results show that our algorithm is competitive with the cutting plane algorithm presented by M. Grotschel et al. (1996) and can be used to solve practically sized problems. (23 Refs)
Subfile: B C
Descriptors: bin packing; graph theory; integer programming; network routing; tree searching
Identifiers: branch-and-price algorithm; **Steiner tree packing** problem; undirected graph; positive integer capacities; nonnegative weights ; node sets; edge capacity limits; total weight minimization; switchbox routing problem; knock-knee model; integer programming; Steiner tree variables; standard test instances; cutting plane approach; STP; column generation
Class Codes: B0260 (Optimisation techniques); B0250 (Combinatorial mathematics); B1130 (General circuit analysis and synthesis methods); C1180 (Optimisation techniques); C1160 (Combinatorial mathematics); C4240 (Programming and algorithm theory); C6120 (File organisation)

Title: A branch-and-price algorithm for the Steiner tree packing problem
Abstract: The paper, deals with the Steiner tree packing problem. For a given undirected graph G=(V,E) with positive integer capacities and nonnegative...
Identifiers: ...Steiner tree packing problem

16/5,K/26 (Item 3 from file: 2) Links
Fulltext available through: ScienceDirect
INSPEC

08183959 **INSPEC Abstract Number:** C2002-03-4260-048
Title: Connected joins in graphs
Author Sebo, A.; Tannier, E.
Author Affiliation: Lab. Leibniz, IMAG, Grenoble, France
Conference Title: Integer Programming and Combinatorial Optimization. 8th International IPCO Conference. Proceedings (Lecture Notes in Computer Science Vol.2081) p. 383-95
Editor(s): Aardal, K.; Gerards, B.
Publisher: Springer-Verlag , Berlin, Germany
Publication Date: 2001 **Country of Publication:** Germany xi+421 pp.
ISBN: 3 540 42225 0 **Material Identity Number:** XX-2001-02092
Conference Title: Integer Programming and Combinatorial Optimization. 8th International IPCO Conference. Proceedings
Conference Date: 13-15 June 2001 **Conference Location:** Utrecht, Netherlands
Language: English **Document Type:** Conference Paper (PA)
Treatment: Practical (P); Theoretical (T)
Abstract: A join in a graph is a set F of edges such that for every circuit C, ; C intersection F; <or= ; C F; . We study the problem of finding a connected join covering a given subset of vertices of the graph, that is a **Steiner tree** which is a **join** at the same time. This turns out to contain the question of finding a T-join of minimum cardinality (or weight) which is, in addition, connected. This last problem is mentioned to be open in a survey of A. Frank (1996), and is motivated by its link to integral packings of T-cuts: if a minimum T-join F is connected, then there exists an integral packing of T-cuts of cardinality ; F; . The problems we deal with are closely related to some known NP-complete problems: deciding the existence of a connected T-join; finding the minimum cardinality of a connected T-**join**; the **Steiner tree** problem; subgraph isomorphism. We also explore some of these connections. (20 Refs)
Subfile: C
Descriptors: computational complexity; computational geometry; graph theory
Identifiers: connected joins; graphs; vertices; Steiner tree; minimum cardinality; integral packing; NP-complete problems; Steiner tree problem; subgraph isomorphism
Class Codes: C4260 (Computational geometry); C4240C (Computational complexity); C1160 (Combinatorial mathematics)

Abstract: ...a connected join covering a given subset of vertices of the graph, that is a **Steiner tree** which is a **join** at the same time. This turns out to contain the question of finding a T... ...the existence of a connected T-join; finding the minimum cardinality of a connected **T-join**; the **Steiner tree** problem; subgraph isomorphism. We also explore some of these connections.

16/5,K/27 (Item 4 from file: 2) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
INSPEC

08163198 **INSPEC Abstract Number:** B2002-03-1110-001
Title: Buffered Steiner trees for difficult instances
Author Alpert, C.J.; Gandham, G.; Hrkic, M.; Jiang Hu; Kahng, A.B.; Lillis, J.; Bao Liu; Quay, S.T.; Sapatnekar, S.S.; Sullivan, A.J.
Author Affiliation: IBM Corp., Austin, TX, USA
Journal: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **Conference Title:** IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. (USA) vol.21, no.1 p. 3-14
Publisher: IEEE ,
Publication Date: Jan. 2002 **Country of Publication:** USA
CODEN: ITCSDI **ISSN:** 0278-0070
SICI: 0278-0070(200201)21:1L.3:BSTD;1-1
Material Identity Number: B959-2002-001
U.S. Copyright Clearance Center Code: 0278-0070/02/$17.00
Conference Title: International Symposium on Physical Design (ISPD)
Conference Date: 2001 **Conference Location:** Sonoma, CA, USA
Document Number: S0278-0070(02)00092-1
Language: English **Document Type:** Conference Paper (PA); Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: With the rapid scaling of integrated-circuit technology, buffer insertion has become an increasingly critical optimization technique in high-performance design. The problem of finding a buffered Steiner tree with optimal delay characteristics has been an active area of research and excellent solutions exist for most instances. However, there exists a class of real "difficult" instances, which are characterized by a large number of sinks (e.g., 20-100), large variations in sink criticalities, nonuniform sink distribution, and varying polarity requirements. Existing techniques are either inefficient, wasteful of buffering resources, or unable to find a high-quality solution. We propose C-tree, a two-level construction that first clusters sinks with common characteristics **together**, constructs low-level **Steiner trees** for each cluster, then performs a timing-driven Steiner construction on the top-level clustering. We show that this hierarchical approach can achieve higher quality solutions with fewer resources compared to traditional timing-driven Steiner trees. (23 Refs)
Subfile: B
Descriptors: buffer circuits; circuit optimisation; integrated circuit design; trees (mathematics)
Identifiers: buffered Steiner tree; integrated circuit design; clustering algorithm; buffer insertion; optimization; delay characteristics; sink distribution; C-tree
Class Codes: B1110 (Network topology); B2570A (Semiconductor integrated circuit design, layout, modelling and testing); B0260 (Optimisation techniques); B0250 (Combinatorial mathematics)

Abstract: ...We propose C-tree, a two-level construction that first clusters sinks with common characteristics **together**, constructs low-level **Steiner trees** for each cluster, then performs a timing-driven Steiner construction on the top-level clustering...

16/5,K/28 (Item 5 from file: 2) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
INSPEC

08067450 **INSPEC Abstract Number:** B2001-11-6150C-043
Title: Efficient algorithms for the multicast trees under the packet-replication restrictions
Author Sung-Jin Chung; Sung-Pil Hong; Hoo-Sang Chung
Author Affiliation: Seoul Nat. Univ., South Korea
Journal: IEICE Transactions on Communications vol.E84-B, no.9 p. 2670-80
Publisher: Inst. Electron. Inf. & Commun. Eng ,
Publication Date: Sept. 2001 **Country of Publication:** Japan
CODEN: ITCMEZ **ISSN:** 0916-8516
SICI: 0916-8516(200109)E84B:9L.2670:EAMT;1-E
Material Identity Number: P711-2001-009
Language: English **Document Type:** Journal Paper (JP)
Treatment: Theoretical (T); Experimental (X)
Abstract: We are concerned with obtaining multicast trees in packet-switched networks such as ATM networks, when there exist constraints on the packet (cell)-replication capabilities of the individual switching nodes. This problem can be formulated as the Steiner tree problem with degree bounds on the nodes, so we call it the degree-constrained Steiner tree problem (DCST). Four heuristic algorithms are proposed: the first is a **combined** version of two well-known **Steiner tree** algorithms, heuristic naive and the shortest path heuristic (SPH), and the second is a relaxation algorithm based on a mathematical formulation of the DCST, and the last two use a tree reconfiguration scheme based on the concept of

'logical link'. We experimentally compare our algorithms with the previous ones in three respects: number of solved instances, objective value or tree cost, and computation time. The experimental results show that there are few instances unsolved by our algorithms, and the objective values are mostly within 5% of optimal. Computation times are also acceptable. (30 Refs)
Subfile: B
Descriptors: asynchronous transfer mode; multicast communication; network topology; packet switching; telecommunication network routing; trees (mathematics)
Identifiers: multicast trees; packet-replication restrictions; packet-switched networks; ATM networks; cell replication; degree-constrained Steiner tree problem; heuristic naive algorithm; shortest path heuristic algorithm; relaxation algorithm; tree reconfiguration; logical link; tree cost; computation time; solved instances
Class Codes: B6150C (Communication switching); B0250 (Combinatorial mathematics); B6150P (Communication network design, planning and routing)

Abstract: ...degree-constrained Steiner tree problem (DCST). Four heuristic algorithms are proposed: the first is a **combined** version of two well-known **Steiner tree** algorithms, heuristic naive and the shortest path heuristic (SPH), and the second is a relaxation...

16/5,K/29 (Item 6 from file: 2) **Links**
Fulltext available through: ScienceDirect
INSPEC

07467923 **INSPEC Abstract Number:** B2000-02-0250-054, C2000-02-1160-069
Title: Vertex-disjoint packing of two Steiner trees: polyhedra and branch-and-cut
Author Uchoa, E.; Poggi de Aragao, M.
Author Affiliation: Dept. de Inf., Pontificia Univ. Catolica do Rio de Janeiro, Brazil
Conference Title: Integer Programming and Combinatorial Optimization. 7th International IPCO Conference. Proceedings p. 439-52
Editor(s): Cornuejols, G.; Burkard, R.E.; Woeginger, G.J.
Publisher: Springer-Verlag , Berlin, Germany
Publication Date: 1999 **Country of Publication:** Germany ix+452 pp.
ISBN: 3 540 66019 4 **Material Identity Number:** XX-1999-01984
Conference Title: Integer Programming and Combinatorial Optimization. 7th International IPCO Conference. Proceedings
Conference Date: 9-11 June 1999 **Conference Location:** Graz, Austria
Language: English **Document Type:** Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: Consider the problem of routing the electrical connections among two large terminal sets in circuit layout. A realistic model for this problem is given by the vertex-disjoint **packing** of two **Steiner trees** (2VPST), which is known to be NP-complete. This work presents an investigation on the 2VPST polyhedra. The main idea is to depart from facet-defining inequalities for a vertex-weighted Steiner tree polyhedra. Some of these inequalities are proven to also define facets for the packing polyhedra, while others are lifted to derive new important families of inequalities, including proven facets. Separation algorithms are also presented. The resulting branch-and-cut code has an excellent performance and is capable of solving problems on grid graphs with up to 10000 vertices and 5000 terminals in a few minutes. (8 Refs)
Subfile: B C
Descriptors: circuit layout; trees (mathematics)
Identifiers: Steiner trees; polyhedra; branch-and-cut; vertex-disjoint packing; NP-complete; Steiner tree polyhedra; packing polyhedra
Class Codes: B0250 (Combinatorial mathematics); B1110 (Network topology); C1160 (Combinatorial mathematics)

Title: Vertex-disjoint packing of two Steiner trees: polyhedra and branch-and-cut
Abstract: ...in circuit layout. A realistic model for this problem is given by the vertex-disjoint packing of two Steiner trees (2VPST), which is known to be NP-complete. This work presents an investigation on the...

16/5,K/30 (Item 7 from file: 2) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
INSPEC

05797132 **INSPEC Abstract Number:** B9412-0250-004, C9412-1290-005
Title: Comparison of formulations and a heuristic for packing Steiner trees in a graph
Author Chopra, S.
Author Affiliation: J.L. Kellogg Graduate Sch. of Manage., Northwestern Univ., Evanston, IL, USA
Journal: Annals of Operations Research vol.50 p. 143-71
Publication Date: Sept. 1994 **Country of Publication:** Switzerland
CODEN: AOREEV **ISSN:** 0254-5330
Language: English **Document Type:** Journal Paper (JP)
Treatment: Applications (A); Theoretical (T)
Abstract: In this paper, we consider the problem of **packing Steiner trees** in a graph. This problem arises during the global routing phase of circuit layout design. We consider various integer programming formulations and rank them according to lower bounds they provide as linear programming (LP) relaxations. We discuss a solution procedure to obtain both lower and upper bounds using one of the LP-relaxations. Computational results to test the effectiveness of our

procedures are provided. (19 Refs)
Subfile: B C
Descriptors: circuit layout; integer programming; linear programming; network routing; operations research; relaxation theory; trees (mathematics)
Identifiers: Steiner trees; packing problem; heuristic; graph theory; global routing; circuit layout design; integer programming; lower bounds; linear programming relaxations; upper bounds
Class Codes: B0250 (Combinatorial mathematics); B0260 (Optimisation techniques); B1130 (General analysis and synthesis methods); C1290 (Applications of systems theory); C1160 (Combinatorial mathematics); C1180 (Optimisation techniques)
Title: Comparison of formulations and a heuristic for packing Steiner trees in a graph
Abstract: In this paper, we consider the problem of packing Steiner trees in a graph. This problem arises during the global routing phase of circuit layout design...

16/5,K/31 (Item 1 from file: 6) **Links**
Fulltext available through: Check for PDF Download Availability and Purchase
NTIS
 NTIS Accession Number: PB94-110947
Twente Workshop on Graphs and Combinatorial Optimization (3rd). Held in Enschede on June 2-4, 1993. Scientific Program
(Memorandum rept)
Faigle, U. ; Hoede, C.
Technische Univ. Twente, Enschede (Netherlands). Faculty of Applied Mathematics.
Corporate Source Codes: 090700007
Report Number: MEMO-1132
May 93 242p
Language: English Document Type: Conference proceeding
Journal Announcement: GRAI9403
See also PB94-110954, N92-24905 and PB93-195568.
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NTIS Prices: PC A11/MF A03
Country of Publication: Netherlands
Partial contents: Almost Distance-Hereditary Graphs; Toughness and Triangle-Free Graphs; Applications of an Algebraic Monge Property; On Special Antimagic Labelings; A Linear Time Algorithm for Finding Tree-Decompositions of Small Treewidth; Cycle Lengths in Non-Bipartite Graphs; **Steiner Trees** and **Packing** Constants in Graph-Metric Spaces; Ordered Matroids and Regular Independence Systems; Generalized Strongly Chordal Graphs; Nordhaus-Gaddum Type Inequalities for the Average Distance of a Graph; Determination of the Rank of Lefschetz Matrices of Products of Posets; Linear Programming in Random Polynomial Time; Polymatroids of the Cone of Boolean Submodular Functions; Bipartite Regular Graphs with Large Diameters.
Descriptors: *Graph theory; *Meetings; Problem solving; Linear programming; Game theory; Scheduling; Matrices; Abstracts; Theorems
Identifiers: *Foreign technology; Combinatorial optimization; Graph coloring; Matroids; NTISTFNPO
Section Headings: 72B (Mathematical Sciences--Algebra, Analysis, Geometry, and Mathematical Logic); 72E (Mathematical Sciences--Operations Research)
...Time Algorithm for Finding Tree-Decompositions of Small Treewidth; Cycle Lengths in Non-Bipartite Graphs; **Steiner Trees** and **Packing** Constants in Graph-Metric Spaces; Ordered Matroids and Regular Independence Systems; Generalized Strongly Chordal Graphs...

16/5,K/32 (Item 2 from file: 6) **Links**
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NTIS
 NTIS Accession Number: N93-28527/8
Packen von Steinerbaeumen: Polyedrische Studien und Anwendung (Packing of Steiner Trees: Polyhedric Studies and Application)
(Ph.D. Thesis)
Martin, A.
Technische Univ. Berlin (Germany, F.R.). Fachgebiet Raumfahrt.
Corporate Source Codes: 030172081; TJ477159
Report Number: ETN-93-93796
1992 196p
Language: German Document Type: Thesis
Journal Announcement: GRAI9321; STAR3111
Text in German.
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NTIS Prices: PC A09/MF A03
Country of Publication: Germany
A formulation to solve the **Steiner tree packing** problem, by means of graph theory, linear algebra polyhedra theory, and

linear programming is developed. The connectivity problem in very large scale integration design, and plane, Manhattan, and knock knee models are presented. Some algorithms for switch box connectivity, such as multicommodity flows in graphs are proposed. Canonic, facet based, and explicit formulation of arborescence polyhedra were examined. The chosen polyhedron was defined as the convex hull of all incidence vectors of Steiner tree packings of a given instance of the problem. A cutting plane algorithm to solve inequalities for polyhedron facet definition with a branch and cut process was developed. Partitioning procedures were realized to solve the separation problem inequalities. The method was applied to problems for the literature.
Descriptors: *Graph theory; *Integrated circuits; *Linear programming; *Optimization; *Packaging; *Trees (Mathematics); Combinatorial analysis; Constraints; Graphs (Charts); Heuristic methods; Homotopy theory; Problem solving; Set theory; Simplex method; Topology
Identifiers: *Foreign technology; Theses; NTISNASAE
Section Headings: 72E (Mathematical Sciences--Operations Research)
Packen von Steinerbaeumen: Polyedrische Studien und Anwendung (Packing of Steiner Trees: Polyhedric Studies and Application)
A formulation to solve the Steiner tree packing problem, by means of graph theory, linear algebra polyhedra theory, and linear programming is developed...

16/5,K/33 (Item 1 from file: 144) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
Pascal

16491488 PASCAL No.: 04-0136014
Effective location-guided tree construction algorithms for small group multicast in MANET
IEEE Infocom 2002 : New York NY, 23-27 June 2002
KAI CHEN; NAHRSTEDT Klara
Computer Science Department, University of Illinois at Urbana-Champaign, Urbana, IL 61801, United States
Conference on computer communicationsIEEE Communications Society. Annual Conference, 21IEEE Computer Society. Annual Conference, 21 (USA) 2002-06-23
Journal: Proceedings - IEEE Infocom, 2002 1180-1189
ISBN: 0-7803-7476-2 ISSN: 0743-166X Availability: INIST-Y 37882; 354000117749251250
No. of Refs.: 24 ref.
Document Type: P (Serial); C (Conference Proceedings) ; A (Analytic)
Country of Publication: United States
Language: English
Group communication has become increasingly important in mobile ad hoc networks (MANET). Current multicast routing protocols in MANET have been shown to have large overhead due to dynamic network topology. To overcome this problem, there is a recent shift towards stateless multicast in small groups (DDM (1)). DDM queries the underlying unicast routing protocol to forward data packets towards members of a multicast group. The multicast distribution tree in DDM is implicit and cannot be controlled by the upper transport and application layers. In this paper, we introduce another small group multicast scheme, based on packet encapsulation, which uses novel packet distribution tree construction algorithms for efficient data delivery. The packet distribution tree is constructed explicitly with the goal of minimizing the overall bandwidth cost of the tree. The tree construction algorithms include a location-guided k-ary (LGK) tree and a location-guided Steiner (LGS) tree. Both of them utilize the geometric locations of the destination nodes as heuristics to compute the trees, and are accompanied by a hybrid location update mechanism to disseminate location information among a group of nodes. Our simulation results show that LGS tree has lower bandwidth cost than LGK tree when the location information of the nodes is up-to-date, and its cost is similar to that of an optimal Steiner multicast tree. When location information of the nodes is out-dated, LGK tree outperforms LGS tree due to its lower computational complexity.
English Descriptors: Localization; Tree algorithm; Multicast; Mobile radiocommunication; Ad hoc network; Wireless telecommunication; Transmission protocol; Multicast protocols; Routing protocols; Network architecture; Topological structure; **Packet** switching; Algorithm performance; **Steiner tree** problem; Heuristic method; Simulation; Performance evaluation; Computational complexity; Data broadcast
French Descriptors: Localisation; Algorithme en arbre; Multidestinataire;

Radiocommunication service mobile; Reseau ad hoc; Telecommunication sans fil; Protocole transmission; Protocole multidestinataire; Protocole routage; Architecture reseau; Structure topologique; Commutation paquet; Performance algorithme; Probleme arbre Steiner; Methode heuristique; Simulation; Evaluation performance; Complexite calcul; Diffusion donnee
Classification Codes: 001D04B04G2; 001D04B03A; 001D04B02D; 001D04B02F

...English Descriptors: Ad hoc network; Wireless telecommunication; Transmission protocol; Multicast protocols; Routing protocols; Network architecture; Topological structure; **Packet** switching; Algorithm performance; **Steiner tree** problem; Heuristic method; Simulation; Performance evaluation; Computational complexity; Data broadcast

16/5,K/34 (Item 2 from file: 144) **Links**
Fulltext available through: ScienceDirect
Pascal

15523738 PASCAL No.: 02-0221029
Multicast routing with bandwidth requirement in the case of incomplete information as a Steiner tree problem
Routage multicast avec information incomplete sur la bande passante vu comme un probleme de Steiner
LEGUESDRON Patrice; LEVENDOVSZKY Janos; MOLNAR Miklos; VEGSO Csaba
CNRS. Institut de recherche en informatique et systemes aleatoires, Rennes, France; Universite de Rennes 1. Institut de recherche en informatique et systemes aleatoires, Rennes, France; Institut national des sciences appliquees de Rennes. Institut de recherche en informatique et systemes aleatoires, Rennes, France; Institut national de recherche en informatique et en automatique. Institut de recherche en informatique et systemes aleatoires, Rennes, France
Journal: Publication interne - IRISA,
2001 18 p., fig., graph. Non-paginated pages/foldouts
ISSN: 1166-8687 Availability: INIST-22588;
354000096886400000
No. of Refs.: 15 ref.
Report No.: IRISA-PI 201-1432
Document Type: P (Serial); R (Report) ; M (Monographic)
Country of Publication: France
Language: English Summary Language: English; French
Dans cet article, nous developpons un nouvel algorithme pour le routage multicast dans les reseaux de communication. Nous transformons le probleme du routage multicast avec contrainte de bande passante lorsque l'information est incomplete en un probleme de Steiner deterministe. Les algorithmes de la methode "tabou" sont ensuite utilises pour s'assurer de la bonne qualite des solutions sous optimales du routage multicast en un temps polynomial.
English Descriptors: Routing algorithm; Network routing; Telecommunication network; Multicast; Incomplete information; Deterministic approach; **Steiner tree** problem; Tabu search; **Packet** switching; Maximum likelihood; Polynomial time; Network architecture; Service quality
French Descriptors: Algorithme routage; Routage reseau; Reseau telecommunication; Multidestinataire; Information incomplete; Approche deterministe; Probleme arbre Steiner; Recherche tabou; Commutation paquet ; Maximum vraisemblance; Temps polynomial; Architecture reseau; Qualite service
Classification Codes: 001D04B02D

English Descriptors: Routing algorithm; Network routing; Telecommunication network; Multicast; Incomplete information; Deterministic approach; **Steiner tree** problem; Tabu search; **Packet** switching; Maximum likelihood; Polynomial time; Network architecture; Service

quality

16/5,K/35 (Item 3 from file: 144) Links
Fulltext available through: USPTO Full Text Retrieval Options
Pascal

14644997 PASCAL No.: 00-0316510
Rank inequalities for packing designs and sparse triple systems
LATIN 2000 : theoretical informatics : Punta del Este, 10-14 April 2000
MOURA L
GONNET Gaston H, ed; PANARIO Daniel, ed; VIOLA Alfredo, ed
Department of Computer Science, University of Toronto, and The Fields Institute for Research in Mathematical Sciences, Canada
Latin American symposium on theoretical informatics, 4 (Punta del Este URY) 2000-04-10
Journal: Lecture notes in computer science, 2000, 1776 105-114
ISBN: 3-540-67306-7 ISSN: 0302-9743 Availability: INIST-16343; 354000080064480110
No. of Refs.: 21 ref.
Document Type: P (Serial); C (Conference Proceedings) ; A (Analytic)
Country of Publication: Germany
Language: English
Combinatorial designs find numerous applications in computer science, and are closely related to problems in coding theory. Packing designs correspond to codes with constant weight; 4-sparse partial Steiner triple systems (4-sparse PSTSs) correspond to erasure-resilient codes able to correct all (except for "bad ones") 4-erasures, which are useful in handling failures in large disk arrays (4,10). The study of polytopes associated with combinatorial problems has proven to be important for both algorithms and theory. However, research on polytopes for problems in combinatorial design and coding theories have been pursued only recently (14,15,17,20,21). In this article, polytopes associated with t-(v, k, A) packing designs and sparse PSTSs are studied. The subpacking and sparseness inequalities are introduced. These can be regarded as rank inequalities for the independence systems associated with these designs. Conditions under which subpacking inequalities define facets are studied. Sparseness inequalities are proven to induce facets for the sparse PSTS polytope; some extremal families of PSTS known as Erdoes configurations play a central role in this proof. The incorporation of these inequalities in polyhedral algorithms and their use for deriving upper bounds on the packing numbers are suggested. A sample of 4-sparse PSTS(v), v <= 16, obtained by such an algorithm is shown; an upper bound on the size of m-sparse PSTSs is presented.
English Descriptors: Computer theory; Combinatorial problem; **Steiner tree** problem; Bin **packing** problem; Polytope
French Descriptors: Informatique theorique; Probleme combinatoire; Probleme arbre Steiner; Probleme remplissage; Polytope
Classification Codes: 001D02A06

English Descriptors: Computer theory; Combinatorial problem; **Steiner tree** problem; Bin **packing** problem; Polytope

16/5,K/36 (Item 4 from file: 144) Links
Fulltext available through: USPTO Full Text Retrieval Options
Pascal

14228689 PASCAL No.: 99-0430150
A polyhedral algorithm for packings and designs
Algorithms : Prague, 16-18 July 1999
MOURA L
NESETRIL Jaroslav, ed

Department of Computer Science, University of Toronto, Toronto, M5S 3G4, Canada
ESA '99 : annual European symposium, 7 (Prague CZE) 1999-07-16
Journal: Lecture notes in computer science,
1999, 1643 462-475
ISBN: 3-540-66251-0 ISSN: 0302-9743 Availability:
INIST-16343; 354000084545070380
No. of Refs.: 18 ref.
Document Type: P (Serial); C (Conference Proceedings) ; A (Analytic)
Country of Publication: Germany; United States
Language: English
We propose a new algorithmic technique for constructing combinatorial designs such as t-designs and packings. The algorithm is based on polyhedral theory and employs the well-known branch-and-cut approach. Several properties of the designs are studied and used in the design of our algorithm. A polynomial-time separation algorithm for clique facets is developed for a class of designs, and an isomorph rejection algorithm is employed in pruning tree branches. Our implementation is described and experimental results are analysed.
English Descriptors: Combinatorial optimization; Bin **packing** problem ; **Steiner tree** problem; Randomised algorithms; Algorithm analysis; Algorithm performance
French Descriptors: Optimisation combinatoire; Probleme remplissage; Probleme arbre Steiner; Algorithme randomise; Analyse algorithme; Performance algorithme
Classification Codes: 001D02A05; 001D01A04

English Descriptors: Combinatorial optimization; Bin **packing** problem ; **Steiner tree** problem; Randomised algorithms; Algorithm analysis; Algorithm performance

16/5,K/37 (Item 5 from file: 144) **Links**
Fulltext available through: SpringerLink USPTO Full Text Retrieval Options
Pascal

12578029 PASCAL No.: 96-0262972
Packing Steiner trees : a cutting plane algorithm and computational results
GROETSCHEL M; MARTIN A; WEISMANTEL R
Konrad-Zuse-Zentrum fuer Informationstechnik Berlin, Takustrasse 7, 14195 Berlin, Germany
Journal: Mathematical programming,
1996, 72 (2) 125-145
ISSN: 0025-5610 CODEN: MHPGA4 Availability: INIST-15655 ; 354000043517070020
No. of Refs.: 22 ref.
Document Type: P (Serial) ; A (Analytic)
Country of Publication: Netherlands
Language: English
In this paper we describe a cutting plane algorithm for the **Steiner tree packing** problem. We use our algorithm to solve some switchbox routing problems of VLSI-design and report on our computational experience. This includes a brief discussion of separation algorithms, a new LP-based primal heuristic and implementation details. The paper is based on the polyhedral theory for the **Steiner tree packing** polyhedron developed in our companion paper (this issue) and meant to turn this theory into an algorithmic tool for the solution of practical problems.
English Descriptors: Graph theory; Trees (mathematics); Polyhedron; Algorithms; Cutting plane method; Separation; Routing; VLSI circuits; Steiner tree problem
French Descriptors: Theorie graphe; Arbre(mathematiques); Polyedre; Algorithme; Methode plan secant; Separation; Acheminement; Circuit VLSI; Probleme arbre Steiner

Classification Codes: 001D01A04

Packing Steiner trees : a cutting plane algorithm
and computational results
In this paper we describe a cutting plane algorithm for the **Steiner tree packing** problem. We use our algorithm to solve some switchbox routing problems of VLSI-design and...
... primal heuristic and implementation details. The paper is based on the polyhedral theory for the **Steiner tree packing** polyhedron developed in our companion paper (this issue) and meant to turn this theory into...

16/5,K/38 (Item 6 from file: 144) **Links**
Fulltext available through: SpringerLink USPTO Full Text Retrieval Options
Pascal

12578028 PASCAL No.: 96-0262971
Packing Steiner trees : polyhedral investigations
GROETSCHEL M; MARTIN A; WEISMANTEL R
Konrad-Zuse-Zentrum fuer Informationstechnik Berlin, Takustrasse 7, 14195 Berlin, Germany
Journal: Mathematical programming, 1996, 72 (2) 101-123
ISSN: 0025-5610 CODEN: MHPGA4 Availability: INIST-15655 ; 354000043517070010
No. of Refs.: 11 ref.
Document Type: P (Serial) ; A (Analytic)
Country of Publication: Netherlands
Language: English
Let G = (V, E) be a graph and T subset = V be a node set. We call an edge set S a Steiner tree for T if S connects all pairs of nodes in T. In this paper we address the following problem, which we call the weighted **Steiner tree packing** problem. Given a graph G = (V, E) with edge weights w SUB e , edge capacities c SUB e , e element of E, and node sets T SUB 1 ,...,T SUB N , find edge sets S SUB 1 ,...,S SUB N such that each S SUB k is a Steiner tree for T SUB k , at most c SUB e of these edge sets use edge e for each e element of E, and the sum of the weights of the edge sets is minimal. Our motivation for studying this problem arises from a routing problem in VLSI-design, where given sets of points have to be connected by wires. We consider the **Steiner tree packing** problem from a polyhedral point of view and define an associated polyhedron, called the **Steiner tree packing** polyhedron. The goal of this paper is to (partially) describe this polyhedron by means of inequalities. It turns out that, under mild assumptions, each inequality that defines a facet for the (single) Steiner tree polyhedron can be lifted to a facet-defining inequality for the **Steiner tree packing** polyhedron. The main emphasis of this paper lies on the presentation of so-called joint inequalities that are valid and facet-defining for this polyhedron. Inequalities of this kind involve at least two Steiner trees. The classes of inequalities we have found form the basis of a branch & cut algorithm. This algorithm is described in our companion paper (in this issue).
English Descriptors: Graph theory; Trees (mathematics); Polyhedron; Inequality; Facet; Algorithms; Cutting plane method; Steiner tree problem
French Descriptors: Theorie graphe; Arbre(mathematiques); Polyedre; Inegalite; Facette; Algorithme; Methode plan secant; Probleme arbre Steiner
Classification Codes: 001D01A04

Packing Steiner trees : polyhedral investigations
... in T. In this paper we address the following problem, which we call the weighted **Steiner tree packing** problem. Given a graph G = (V, E) with edge weights w SUB e , edge capacities...
... design, where given sets of points have to be connected by wires. We consider the **Steiner tree packing** problem from a

polyhedral point of view and define an associated polyhedron, called the **Steiner tree packing** polyhedron. The goal of this paper is to (partially) describe this polyhedron by means of...
... the (single) Steiner tree polyhedron can be lifted to a facet-defining inequality for the **Steiner tree packing** polyhedron.
The main emphasis of this paper lies on the presentation of so-called joint
...

16/5,K/39 (Item 1 from file: 34) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
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10137620 **Genuine Article#:** 489JW **Number of References:** 23
A branch-and-price algorithm for the Steiner tree packing problem
Author: Jeong GW; Lee K; Park S (REPRINT) ; Park K
Corporate Source: Korea Adv Inst Sci & Technol,Dept Ind Engn, Yusong Gu,373-1 Gusong Dong/Taejon 305701//South Korea/ (REPRINT); Korea Adv Inst Sci & Technol,Dept Ind Engn, Yusong Gu,Taejon 305701//South Korea/; Elect & Telecommun Res Inst,Yusong Gu,Taejon 303350//South Korea/; Korea Telecom,Telecommun Networks Lab, Yusong Gu,Taejon 305390//South Korea/
Journal: COMPUTERS & OPERATIONS RESEARCH , 2002 , V 29 , N3 (MAR) , P 221-241
ISSN: 0305-0548 **Publication date:** 20020300
Publisher: PERGAMON-ELSEVIER SCIENCE LTD , THE BOULEVARD, LANGFORD LANE, KIDLINGTON, OXFORD OX5 1GB, ENGLAND
Language: English **Document Type:** ARTICLE
Geographic Location: South Korea
Journal Subject Category: COMPUTER SCIENCE, INTERDISCIPLINARY APPLICATIONS; ENGINEERING, INDUSTRIAL; OPERATIONS RESEARCH & MANAGEMENT SCIENCE
Abstract: This paper deals with the **Steiner tree packing** problem. For a given undirected graph G = (V, E) with positive integer capacities and non-negative weights on its edges, and a list of node sets (nets), the problem is to find a connection of nets which satisfies the edge capacity limits and minimizes the total weights. We focus on the switchbox routing problem in knock-knee model and formulate this problem as an integer programming using Steiner tree variables. We develop a branch-and-price algorithm. The algorithm is applied on some standard test instances and we compare the performances with the results using cutting-plane approach. Computational results show that our algorithm is competitive to the cutting plane algorithm presented by Grotschel et al. and can be used to solve practically sized problems.
Descriptors--Author Keywords: **Steiner tree packing** problem (STP) ; VLSI design ; branch-and-price ; column generation
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SAIT M, 1995, VLSI PHYSICAL DESIGN
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SAVELSBERGH M, 1997, V45, P831, OPER RES
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A branch-and-price algorithm for the Steiner tree packing problem
Abstract: This paper deals with the Steiner tree packing problem. For a given undirected graph G = (V, E) with positive integer capacities and non...

16/5,K/40 (Item 2 from file: 34) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
SciSearch(R) Cited Ref Sci

09024512 **Genuine Article#:** 358AV **Number of References:** 39
Provably good global routing of integrated circuits
Author: Lengauer T (REPRINT) ; Lugering M
Corporate Source: GERMAN NATL RES CTR INFORMAT TECHNOL,SCHLOSS BIRLINGHOVEN/ST AUGUSTIN//GERMANY/ (REPRINT); UNIV BONN,DEPT COMP SCI/D-5300 BONN//GERMANY/
Journal: SIAM JOURNAL ON OPTIMIZATION , 2000 , V 11 , N1 (AUG 24) , P 1-30
ISSN: 1052-6234 **Publication date:** 20000824
Publisher: SIAM PUBLICATIONS , 3600 UNIV CITY SCIENCE CENTER, PHILADELPHIA, PA 19104-2688
Language: English **Document Type:** ARTICLE
Geographic Location: GERMANY
Subfile: CC PHYS--Current Contents, Physical, Chemical & Earth Sciences
Journal Subject Category: MATHEMATICS, APPLIED
Abstract: This paper investigates the global routing problem for integrated circuits. We introduce a formulation on the basis of integer programming which minimizes the routing area among a limited set of Steiner trees for each net. Indeed, the involved cost function depends on the channel density of the routing which has a direct influence on the routing area.

Our methods for solving the global routing problem employ local search heuristics, sequential routing, genetic routing, and randomized procedures. Our methods for computing lower bounds are based on linear and Lagrange relaxation. An analysis on the tightness of the bounds indicates that the difference between the cost of the optimal integer solutions and the cost of the optimal fractional solutions is only a small number of tracks in practice. Moreover, the analysis leads to the concept of linear preprocessing by which we exclude a large number of high-cost solutions.

We introduce several versions of preprocessing, one of which preserves the opportunity of obtaining a globally optimal solution in general; all of them do so in practice. Linear preprocessing enables us to solve problem instances with several thousand nets provably optimal or at least provably close to optimal.

All methods have been implemented in the software package ERIDANUS. We present computational results.

The global routing problem assumes the placement of the chip components to be fixed. An extension of the problem, which we call global layout of integrated circuits, allows the placement to be variable and searches for a placement that minimizes the routing area among a limited set of alternatives. We show that the results concerning the global routing problem can be easily extended to global layout.
Descriptors--Author Keywords: routing ; integer programming ; integrated circuits ; combinatorial optimization
Identifiers-- KeyWord Plus(R): **PACKING STEINER TREES**; ROUTER; ALGORITHM; DESIGN
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Identifiers-- ...**PACKING STEINER TREES**; ROUTER; ALGORITHM; DESIGN

16/5,K/41 (Item 3 from file: 34) Links
Fulltext available through: SpringerLink USPTO Full Text Retrieval Options
SciSearch(R) Cited Ref Sci

08567304 **Genuine Article#:** 302AR **Number of References:** 8
Gaps in convex disc packings with an application to 1-Steiner Minimum Trees
Author: Swanepoel KJ (REPRINT)
Corporate Source: UNIV PRETORIA,DEPT MATH & APPL MATH/ZA-0002 PRETORIA//SOUTH AFRICA/ (REPRINT)
Journal: MONATSHEFTE FUR MATHEMATIK , 2000 , V 129 , N3 , P 217-226
ISSN: 0026-9255 **Publication date:** 20000000
Publisher: SPRINGER-VERLAG WIEN , SACHSENPLATZ 4-6, PO BOX 89, A-1201 VIENNA, AUSTRIA
Language: English **Document Type:** ARTICLE
Geographic Location: SOUTH AFRICA
Subfile: CC PHYS--Current Contents, Physical, Chemical & Earth Sciences
Journal Subject Category: MATHEMATICS
Abstract: We show that if six translates of a convex disc C all touch C, and no two of the translates have interior points in common, then there are never more than two gaps, i.e., consecutive non-touching pairs of translates. We also characterize the configurations where there are two, one or no gaps. This result is then applied to show that the Steiner point in a 1-Steiner Minimum Tree in a normed plane has degree at most five if the unit ball is not an affine regular hexagon (where Steiner points of degree six exist).
Descriptors--Author Keywords: convex disc ; **packing ; Steiner minimal tree ; Steiner minimum tree** ; Hadwiger number
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16/5,K/42 (Item 4 from file: 34) Links
Fulltext available through: custom link USPTO Full Text Retrieval Options
SciSearch(R) Cited Ref Sci

08135852 **Genuine Article#:** 250FG **Number of References:** 19
Routing through virtual paths in layered telecommunication networks
Author: Dahl G (REPRINT) ; Martin A; Stoer M
Corporate Source: UNIV OSLO,DEPT MATH, POB 1080/N-0316 OSLO//NORWAY/ (REPRINT); KONRAD ZUSE ZENTRUM INFORMAT TECH,/D-10711 BERLIN//GERMANY/; TELENOR,/N-2027 KJELLER//NORWAY/
Journal: OPERATIONS RESEARCH , 1999 , V 47 , N5 (SEP-OCT) , P 693-702
ISSN: 0030-364X **Publication date:** 19990900
Publisher: INST OPERATIONS RESEARCH MANAGEMENT SCIENCES , 901 ELKRIDGE LANDING RD, STE 400, LINTHICUM HTS, MD 21090-2909
Language: English **Document Type:** ARTICLE
Geographic Location: NORWAY; GERMANY
Subfile: CC ENGI--Current Contents, Engineering, Computing & Technology;
Journal Subject Category: OPERATIONS RESEARCH & MANAGEMENT SCIENCE
Abstract: We study a network configuration problem in telecommunications where one wants to set up paths in a capacitated network to accommodate given point-to-point traffic demand. The problem is formulated as an integer linear programming model where 0-1 variables represent different paths. An associated integral polytope is studied, and different classes of facets are described. These results are used in a cutting plane algorithm. Computational results for same realistic problems are reported.
Identifiers-- KeyWord Plus(R): **PACKING STEINER TREES**; ALGORITHM
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Identifiers-- ...**PACKING STEINER TREES**; ALGORITHM

16/5,K/43 (Item 5 from file: 34) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
SciSearch(R) Cited Ref Sci

06879740 **Genuine Article#:** ZY725 **Number of References:** 14
Switchbox routing in VLSI design: Closing the complexity gap
Author: Hartmann S (REPRINT) ; Schaffter MW; Schulz AS
Corporate Source: TECH UNIV BERLIN,FACHBEREICH MATH, MA 6-1, STR 17 JUNI 136/D-10623 BERLIN//GERMANY/ (REPRINT)
Journal: THEORETICAL COMPUTER SCIENCE , 1998 , V 203 , N1 (AUG 6) , P 31-49
ISSN: 0304-3975 **Publication date:** 19980806
Publisher: ELSEVIER SCIENCE BV , PO BOX 211, 1000 AE AMSTERDAM, NETHERLANDS
Language: English **Document Type:** ARTICLE
Geographic Location: GERMANY
Subfile: CC ENGI--Current Contents, Engineering, Computing & Technology
Journal Subject Category: COMPUTER SCIENCE, THEORY & METHODS
Abstract: The design of integrated circuits has achieved a great deal of attention in the last decade. In the routing phase, there have survived two unsolved layout problems that are important from both the theoretical and the practical point of view. Up to now, switchbox routing has been known to be solvable in polynomial time when there are only 2-terminal nets, and to be NP-complete in case there exist nets involving at least five terminals. Our main result is that this problem is NP-complete even if no net has more than three terminals. Hence, from the theoretical perspective, the switchbox routing problem is completely settled.

The NP-completeness proof is based on a reduction from a special kind of the satisfiability problem. It also is possible to adopt our construction to channel routing implying that this problem is NP-complete, even if each net does not consist of more than five terminals. This improves upon a result of Sarrafzadeh who proved the NP-completeness in case of nets with no more than six terminals. (C) 1998-Elsevier Science B.V. All rights reserved.
Descriptors--Author Keywords: VLSI design ; switchbox routing ; NP-completeness ; **Steiner tree packing**
Identifiers-- KeyWord Plus(R): CHANNEL
Cited References:
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16/5,K/44 (Item 6 from file: 34) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
SciSearch(R) Cited Ref Sci

04874535 **Genuine Article#:** UN919 **Number of References:** 38
PLANAR CLOCK ROUTING FOR HIGH-PERFORMANCE CHIP AND PACKAGE CO-DESIGN
Author: ZHU Q; DAI WWM
Corporate Source: INTEL CORP,INTEL DEV LABS/SANTA CLARA//CA/95062; UNIV CALIF SANTA CRUZ,DEPT COMP ENGN/SANTA CRUZ//CA/95064
Journal: IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS , 1996 , V 4 , N2 (JUN) , P 210-226
ISSN: 1063-8210
Language: ENGLISH **Document Type:** ARTICLE
Geographic Location: USA
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC; COMPUTER SCIENCE, HARDWARE & ARCHITECTURE

Abstract: A new concept of chip and package co-design for the clock network is presented in this paper, We propose a two-level clock distribution scheme which partitions the clock network into two levels, First, the clock terminals are partitioned into a set of clusters, For each cluster, a local on-chip clock tree is used to distribute the clock signal from a locally inserted buffer to terminals inside this cluster, The clock signal is then distributed from the main clock driver to each of local buffers by means of a global clock tree, which is a planar tree with equal path lengths, With the hip chip area I/O. attachment, the planar global clock tree can be put on a dedicated package layer, The interconnect on the package layer has two to four order smaller resistance than that on the chip layer, The main contribution of this paper is a novel algorithm to construct a planar clock tree with equal path lengths-the length of the path from the clock source to each destination is exactly the same, In addition, the path length from the source to destinations is minimized.
Descriptors--Author Keywords: CLOCK DISTRIBUTION ; CLOCK ROUTING ; CLOCK TREE ; CHIP AND PACKAGE CO-DESIGN ; HIP CHIP ; INTERCONNECT ; **PACKAGE** ; PLANAR ROUTING ; **STEINER TREE**
Research Fronts: 94-5198 001 (PERFORMANCE-DRIVEN GLOBAL ROUTING ALGORITHM FOR GATE ARRAY; RISC WORKSTATION PACKAGING)
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16/5,K/45 (Item 7 from file: 34) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
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04547891 **Genuine Article#:** TR447 **Number of References:** 11
PACKING STEINER TREES - FURTHER FACETS
Author: GROTSCHEL M; MARTIN A; WEISMANTEL R
Corporate Source: KONRAD ZUSE ZENTRUM BERLIN/D-10711 BERLIN//GERMANY/
Journal: EUROPEAN JOURNAL OF COMBINATORICS , 1996 , V 17 , N1 (JAN) , P 39-52
ISSN: 0195-6698
Language: ENGLISH **Document Type:** ARTICLE
Geographic Location: GERMANY
Subfile: SciSearch
Journal Subject Category: MATHEMATICS
Abstract: In this paper we continue the investigations in [3] for the **Steiner tree packing** polyhedron. We present several new classes of valid inequalities and give sufficient (and necessary) conditions for these inequalities to be facet-defining. It is intended to incorporate these inequalities into an existing cutting plane algorithm that is applicable to practical

problems arising in the design of electronic curcuits. (C) 1995 Academic Press Limited
Identifiers-- KeyWords Plus: CHANNEL
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PACKING STEINER TREES - FURTHER FACETS
Abstract: In this paper we continue the investigations in [3] for the Steiner tree packing polyhedron. We present several new classes of valid inequalities and give sufficient (and necessary) conditions...

16/5,K/46 (Item 1 from file: 434) Links
SciSearch(R) Cited Ref Sci

08632995 **Genuine Article#:** M2796 **Number of References:** 32
GREEDY - A NEW STARTING SET PROCEDURE
Author: SCHAGEN JD; SCHENK H
Corporate Source: UNIV AMSTERDAM,CRYSTALLOG LAB,NIEUWE ACHTERGRACHT 166/1018 WV AMSTERDAM//NETHERLANDS/
Journal: ZEITSCHRIFT FUR KRISTALLOGRAPHIE , 1987 , V 179 , N1-4 , P 97-111
Language: ENGLISH **Document Type:** ARTICLE
Geographic Location: NETHERLANDS
Subfile: SciSearch; CC PHYS--Current Contents, Physical, Chemical & Earth Sciences
Journal Subject Category: CRYSTALLOGRAPHY
Research Fronts: 86-1145 001 (MULTIWAVELENGTH ANOMALOUS DIFFRACTION DATA IN MACROMOLECULAR CRYSTALLOGRAPHY; RECOVERING PHASE INFORMATION; INTERSTITIAL RETINOL- **BINDING** PROTEIN (IRBP))
86-5811 001 (**STEINER** MINIMAL-**TREES**; COMBINATORIAL OPTIMIZATION; MINIMAL SPANNING TREE)
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Research Fronts: 86-1145 001 (MULTIWAVELENGTH ANOMALOUS DIFFRACTION DATA IN MACROMOLECULAR CRYSTALLOGRAPHY; RECOVERING PHASE INFORMATION; INTERSTITIAL RETINOL- **BINDING** PROTEIN (IRBP))

86-5811 001 (**STEINER** MINIMAL-TREES; COMBINATORIAL OPTIMIZATION; MINIMAL SPANNING TREE)

16/5,K/47 (Item 1 from file: 95) **Links**
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TEME-Technology & Management

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Planar clock routing for high performance chip and package co-design
(Planares Taktrouting fuer einen Hochleistungschip)
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Dev. Labs., Intel Corp., Santa Clara, CA, USA
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Abstract:
A new concept of chip and package co-design for the clock network is presented in this paper. We propose a two level clock distribution scheme which partitions the clock network into two levels. First, the clock terminals are partitioned into a set of clusters. For each cluster, a local on-chip clock tree is used to distribute the clock signal from a locally inserted buffer to terminals inside this cluster. The clock signal is then distributed from the main clock driver to each of local buffers by means of a global clock tree, which is a planar tree with equal path lengths. With the flip chip area I/O attachment, the planar global clock tree can be put on a dedicated package layer. The interconnect on the package layer has two to four order smaller resistance than that on the chip layer. The main contribution of this paper is a novel algorithm to construct a planar clock tree with equal path lengths-the length of the path from the clock source to each destination is exactly the same. In addition, the path length from the source to destinations is minimized.
Descriptors: GRAND SCALE INTEGRATION; CIRCUIT CAD; INTEGRATED CIRCUIT PACKAGING; CHIPS--SEMICONDUCTORS; CLOCK FREQUENCY; CLUSTER FORMING; FLIP CHIP DEVICES; I O UNIT; ALGORITHM; DIGITAL ICS; TREE STRUCTURE; NETWORK STUCTURE--ELECTRIC; INTEGRATED CIRCUIT DESIGN; INTEGRATED CIRCUIT INTERCONNECTIONS; NETWORK ROUTING
Identifiers: PLANAR CLOCK ROUTING; TWO LEVEL CLOCK DISTRIBUTION SCHEME; LOCAL ON CHIP CLOCK TREE; LOCALLY INSERTED BUFFER; CLOCK DRIVER; LOCAL BUFFERS; GLOBAL CLOCK TREE; EQUAL PATH LENGTHS; DEDICATED **PACKAGE** LAYER; **STEINER TREE**; TAKTSIGNALVERTEILUNG; Taktrouting; Hochleistungs-Chip
Identifiers: ...TREE; LOCALLY INSERTED BUFFER; CLOCK DRIVER; LOCAL BUFFERS; GLOBAL CLOCK TREE; EQUAL PATH LENGTHS; DEDICATED **PACKAGE** LAYER; **STEINER TREE**; TAKTSIGNALVERTEILUNG; Taktrouting; Hochleistungs-Chip